Design automation towards reliable analog integrated circuits

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Abstract— **Reliability is becoming one of the major concerns in designing integrated circuits in nanometer CMOS technologies. Problems related to degradation mechanisms like NBTI or soft breakdown, as well as increased external interference such as caused by crosstalk and EMI, cause time-dependent circuit performance degradation. Variability only makes these things more severe. This creates a need for innovative design techniques and design tools that help designers coping with these reliability and variability problems. This tutorial paper gives a brief description of design tools for the efficient analysis and identification of reliability problems in analog circuits, as a first step towards the automated design of guaranteed reliable analog circuits.**

1 INTRODUCTION

The evolution towards nanometer CMOS technologies (90 nm, 65 nm, 45 nm and below) [1] has enabled the design of highly integrated systems for consumer-market applications such as telecom and multimedia. These integrated systems are increasingly mixed-signal designs with embedded high-performance analog or mixed-signal blocks and possibly sensitive RF frontends.

The use of CMOS nanometer technologies however also brings significant challenges for circuit design that were not encountered before. Such challenges include [2]:

- managing the ever increasing design complexities in tightening time-to-market constraints;
- the increasing variability of technology parameters, causing mismatch and yield problems;
- worsening degradation mechanisms (e.g. NBTI, Hot Carriers, Soft Breakdown) and increasing reliability constraints such as EMC/EMI regulations.

This tutorial paper focuses on reliability problems encountered in analog integrated circuits in nanometer CMOS technologies, and describes design tools for the analysis of these phenomena. The paper is organized as follows. Section 2 briefly describes the impact of variability, reliability and electromagnetic interference on analog circuit performance degradation. Section 3 outlines an approach for the reliability analysis and the detection of reliability weak spots in analog circuits. The interaction between variability and degradation is emphasized. Finally, section 4 provides conclusions.

2 ANALOG CIRCUIT PERFORMANCE DEGRADATION

2.1 Variability and mismatch

Many non-idealities in analog circuits originate from random and systematic errors in the implementation of the circuit. These errors represent the time-independent reliability problems in a circuit. Random errors, usually denoted as variability, are the result of the stochastic nature of many physical processes that take place during the fabrication of integrated circuits, such as line edge roughness and random dopant fluctuations. In analog circuits device mismatch between identically designed devices is a key limitation to the accuracy of the circuits (e.g. data converters, filters, etc.).

Fortunately, although mismatch is statistical in the sense that it is unknown before fabrication and therefore random at design time, it is fixed after fabrication. Therefore, all such static time-independent errors can to large extent be compensated for after fabrication using post-fabrication calibration methods. These typically utilize the huge potential of digital circuits which basically are cheaply and abundantly available in nanometer CMOS technologies. The same compensation concept can also be applied to other non-idealities of analog circuits, resulting in the general paradigm of digitally assisted analog circuits [3].

2.2 Time-dependent degradation

Time-dependent degradation effects will cause a change of the transistor parameters (V_T, γ, r_o) as a function of time and therefore might turn an initially fully functional circuit into a less or even non-functional circuit over time [2]. This degradation depends on the stress applied to the device, i.e. the voltages and currents applied to the transistor. Fig. 1 qualitatively indicates the impact of these mechanisms on the I_{DS}-V_{DS} characteristic of a MOS device for an arbitrary stress time. Some of the most important degradation mechanisms will now be discussed in some more detail.

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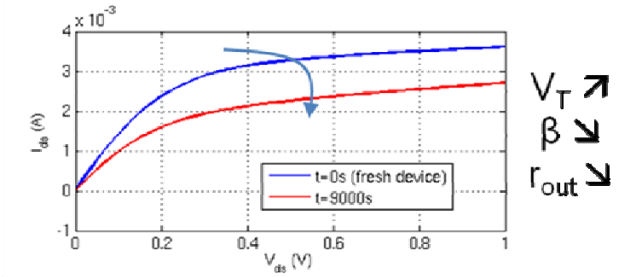

Fig. 1. Time-dependent variation of the characteristics of a transistor due to Hot-Carrier and NBTI degradation [2].

2.2.1 Time-dependent dielectric breakdown

In nanometer CMOS the strong electric field across the gate oxide can cause oxide damage resulting in dielectric breakdown (BD). BD is a local phenomenon, and results in an increase of the transistor gate current. During the degradation process different BD modes can be distinguished. For oxide thicknesses below 5nm, HBD can be preceded by soft breakdown (SBD) [4], which can be observed as a partial loss of the dielectric properties, resulting in a smaller increase of the gate current compared to hard breakdown [5,6].

The probability to have n SBD defects at time t can be described with a Poisson distribution [7]:

$$P_n(t) = \frac{1}{n!}\left(\frac{t}{t_{SBD}}\right)^{\beta n} \exp\left(-\left(\frac{t}{t_{SBD}}\right)^{\beta}\right) \quad (1)$$

where β is a process-dependent parameter with typical value 1.2 and t_{SBD} depends on the transistor area and the applied stress voltage. Formula (1) is however only valid for fixed stress voltages, and while a circuit is aging, transistor operating points might change due to aging-induced shifting transistor parameters. A dynamic SBD model, including support for changing operating points, is therefore required. An approach for stochastically analyzing SBD is presented in [8]. Because SBD is a stochastic effect, it may result in an increasing asymmetry over time between identical devices, hence resulting in time-dependent mismatch and offset in analog circuits.

2.2.2 Hot-carrier injection

A second degradation phenomenon is Hot Carrier Injection (HCI), which manifests itself mainly as a threshold voltage shif, and some degradation of carrier mobility and a change of output resistance [9,10]. During hot carrier stress, which consists of a large electric field near the drain end of a transistor in saturation, hot carriers are produced. These carriers introduce both oxide and interface traps (near the drain) and a substrate current. As holes are much 'cooler' than electrons, hot carrier effects in nMOS devices are proven to be more significant than in pMOS devices [11]. Removal of the stress anneals some of the interface traps, resulting in partial recovery. But as these traps are only present at the drain junction of the transistor, this recovery is negligible in comparison to NBTI relaxation.

HCI degradation is typically modeled with a power law dependence on the stress time t [10]:

$$\Delta V_T = A(V_{GS}, V_{DS}, T, W, L...)\, t^n \quad (2)$$

where n typically is around 0.45 and the function $A(...)$ depends on the applied voltages, the temperature but also on the transistor width and length. Due to hot carrier degradation, transistor characteristics and therefore circuit performance degrade over time. Therefore, tools need to be developed to analyze this problem and to identify possible reliability problems in a circuit during the design stage. Such analysis tool will be described in section 3.

2.2.3 Negative bias temperature instability

Negative Bias Temperature Instability (NBTI) has an increasingly adverse impact on nanometer CMOS technology [12]. NBTI is typically seen as a threshold voltage shift after a negative bias has been applied to a MOS gate at elevated temperature, mainly affecting pMOS transistors [13]. Degradation of channel carrier mobility is also observed. The NBTI degradation is typically represented as following a power law with stress time, similar to equation (2) but with a different exponent n which typically is around 0.16 and with a different function $A(...)$.

A peculiar property of the NBTI mechanism is the so-called relaxation or recovery of the degradation immediately after the stress voltage has been reduced [14]. This relaxation behavior greatly complicates the evaluation of NBTI, its modeling, and extrapolating its impact on circuitry. The relaxation of the threshold voltage shift has been observed to have approximately a logarithmic time dependence and spanning times from microseconds to days [15]. It currently appears that NBTI degradation does not fully recover. A complete model of NBTI useful for circuit analysis in a SPICE-like simulator is presented in [16].

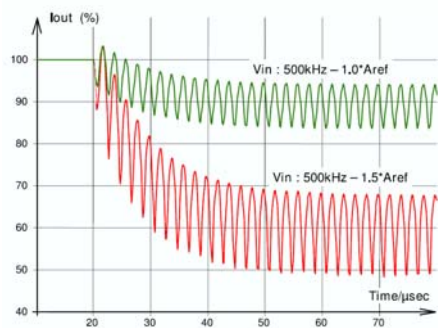

Fig. 2. Electromagnetic interference can shift the DC operating point of a circuit (I_{out} in the example at hand) and thereby ruin circuit functionality [17].

2.2.4 Electromagnetic interference

Electromagnetic Compatibility (EMC) is another rising challenge in current IC designs. The higher switching speeds and the explosion of wireless traffic generated by mobile phones, wireless networks, Bluetooth transceivers, etc... can severely affect the performance of devices in a

common electromagnetic environment. In addition, the reduced supply voltage and the increased number of communication interfaces decrease the immunity to interference. EMC is defined as the ability to function satisfactorily in a common electromagnetic environment without introducing intolerable electromagnetic disturbance to anything in that environment. It is an important design requirement in safety-critical applications such as automotive and biomedical, and is typically enforced through EMC regulations.

In analog circuits, the shift of the DC operating point due to electromagnetic interference (EMI) is identified as one of the major causes of failure in susceptibility tests [17,18]. In this sense EMI can be considered as an environment-induced degradation phenomenon. Fig. 2 illustrates the disastrous effect of interference on the output current of a current reference [17]: due to circuit nonlinearity the mean output current I_{out} shifts to a lower value over time rather than staying constant. The error in output current depends on the amplitude and the frequency of the EMI signal. It is therefore important to simulate the immunity of the circuit and to indicate the EMC problem spots in the design before tapeout, using dedicated EMC analysis tools such as for instance presented in [19].

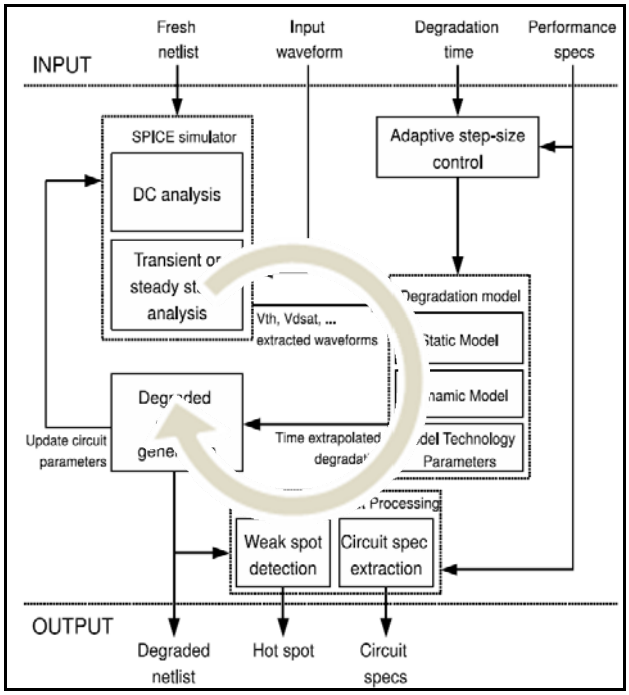

Fig. 3. Flow diagram of efficient nominal degradation analysis of analog circuits [20].

3 Reliability Analysis of Analog Integrated Circuits

Due to the impact of time-dependent degradation on integrated circuits, it is important to analyze quantitatively the impact of the above degradation phenomena and to identify potential reliability problems at design time, so that – if needed – the design can be modified to guarantee correct functionality and performance over the lifetime of the electronic product. Therefore, proper reliability simulation and analysis tools are needed for analog circuits, as a first step towards more automated design for reliability.

In [20] a novel and very efficient method for reliability simulation is presented, offering more correct results than commercial tools. It uses a short transient simulation that provides accurate information about the stress at every circuit node, while a degradation extrapolation ensures a fast simulation result. Fig. 3 gives a schematic representation of this reliability simulation algorithm. The input to the simulator is a fresh (i.e. unstressed) netlist. A transient simulation over a short time period is performed on the input netlist. As circuit input a periodic time-varying signal is applied. The impact of completely arbitrary (i.e. non-periodic) input signals can only be calculated using a transient analysis over the entire operating period of the circuit, which obviously is not very feasible. Once the stress pattern on every transistor node is calculated from this initial simulation, it is extracted and passed on to a degradation model, which extrapolates the transistor degradation over a longer time period. This results in a shift in the operating point, requiring the same steps to be iterated a number of times. Finally, a degraded version of the netlist is created as an output. A designer can use this output netlist to study the impact of degradation on the product lifetime and to identify the reliability weak spots in the design.

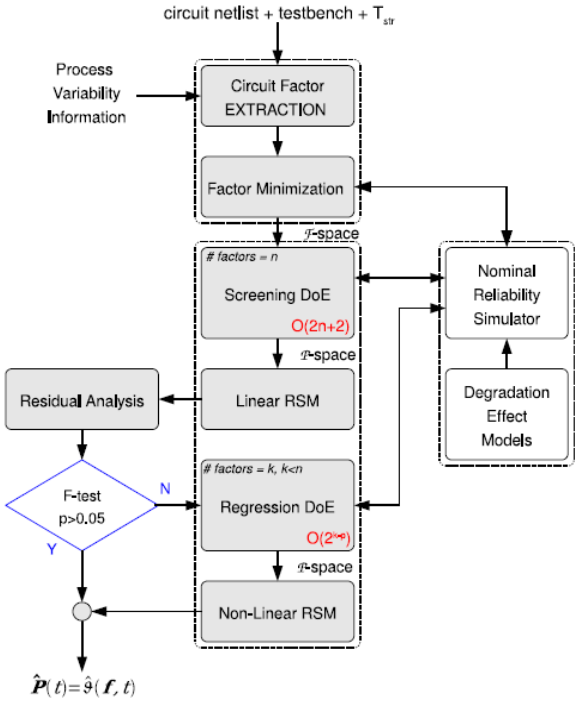

Fig.4. Variability-aware reliability analysis of analog circuits with parameter pre-screening and response surface modeling to achieve high efficiency [21].

One of the important observations during the simulation experiments is that degradation is impacted a lot by variability, i.e. by the statistical variations of the process parameters. This implies that the above reliability analysis must be repeated for a large number of statistical circuit instances. A crude approach is to solve this with Monte-Carlo analysis [20]. However, to avoid the time-consuming Monte-Carlo analysis, a more efficient variability-aware reliability analysis is presented in [21] and shown in Fig. 4. Efficiency in this flow is obtained by the pre-screening of important statistical parameters and the efficient calculation using response surface models built with design of experiment techniques. As can be seen, this flow calls the nominal reliability analysis tool of Fig. 3 as internal subroutine.

To illustrate the interaction between reliability and variability, an LC-VCO is analyzed in a 90 nm technology [20]. Large voltages at the drains of the cross-coupled transistor pair cause the transistors to suffer from hot-carrier degradation. Fig. 5 shows the effect of degradation on the oscillator output voltage which decreases significantly over time, hence limiting the lifetime of the product. Fig. 5 clearly shows the failure time dispersion of the oscillator due to local and global statistical variations of the transistor parameters.

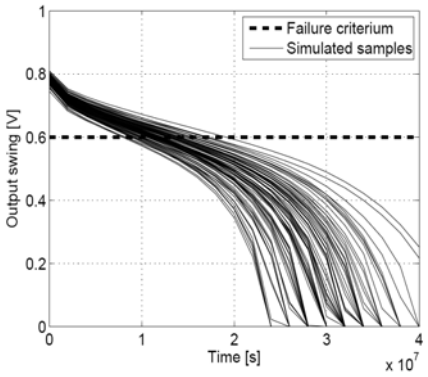

Fig. 5. Variability-induced dispersion of the time to failure due to decreasing output voltage of an LC-VCO [20].

4 Conclusions

CMOS technology is evolving deeper and deeper into the nanometer era, enabling on the one hand the realization of highly integrated systems, but on the other hand causing increasing variability and reliability problems. This tutorial paper has given a brief overview of reliability problems in analog integrated circuits, such as soft breakdown, hot carriers or NBTI, which cause time-dependent degradation of the circuits. Also the effect of electromagnetic interference has been discussed. In addition, efficient variability-aware analysis tools have been presented for the analysis and identification of reliability problems in analog circuits, as an important step towards automated analog design for reliability. All this has been illustrated with some circuit examples.

Acknowledgments

The authors acknowledge the financial support of FWO, IWT SBO and EU FP7 for different parts of this work.

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