Board Driven I/O Planning & Optimization

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I. INTRODUCTION

The vast majority of IC’s that go into production must reside on a Printed Circuit Board (PCB). Unfortunately, the design and layout of this PCB is often an afterthought and never considered in the planning of the chip itself. The result is a PCB that is very difficult to complete on a minimal number of layers and signal integrity is often compromised. This often creates a huge bottleneck in the time it takes a chip to ship in volume and often cuts into a company’s profit margin. This bottleneck (and additional cost) can be greatly reduced by implementing a cross-domain co-design methodology that considers the physical layout requirements of the PCB (without looking over the package substrate) in the context of floor-planning the chip.

The PCB is a significant cost element of the final product. Therefore, a great deal of time and effort is spent on optimizing the PCB for layer reduction to drive down cost and signal quality for maximum performance. The board designer spends a considerable amount of this time trying to un-ravel the rat nest of connections between devices during the placement stage of the layout. Since this un-raveling of interconnect only takes place between the board level pins (with very limited swapping capabilities), the final placement typically has a large number of tangled signals that need to be routed on the fewest possible layers. This tangled mess is often too much for an auto-router to handle, leading to the PCB designer to spend weeks or months hand routing the board. In addition, the longer interconnects on the PCB can adversely affect the overall performance of the system.

If considered early in the process, the PCB layout can be used to guide I/O placement and floor-planning of the chip without any adverse effects on the performance of the device. The outcome would be a “PCB aware” IC (and its package) driving onto a PCB with fewer layers, designed in less time, leading to a significant cost savings and shorter time to market.

This paper outlines a methodology for using basic PCB layout data to plan and optimize interconnect and I/O placement for the chip and its package.

II. PROPOSAL

A. The building blocks to co-design

With the growth in multi-die packaging (SiP), 3D-IC (TSV) and the increased I/O count on many of today’s SoCs, several companies are starting to recognize the value of cross-team collaboration between the IC, package and PCB design groups. These types of designs are driving engineers to reconsider how they plan/automate the I/O placement on their chips. In some instances, informal design flows based on multiple EDA design tools are starting to be pieced together. This is a step in the right direction, however without a central repository for the data or accurate device models, design intent is often misinterpreted or lost and redundancy is often introduced into the flow.

For an example of an inaccurate device model, we can start with the IC itself. Today, there are no formal standards for passing IC layout data to/from the package design team. Typically, an abstract of the die with a very limited set of design data is generated from the IC place & route tool. This die abstract typically only contains pad locations, signal names and overall physical size. While this may be enough information for physical design of the package, this is not enough data to implement an intelligent co-design methodology. To implement a productive board driven I/O methodology a more accurate model of the die is required.

One proposal is to develop and standardize on a Virtual Die Model (VDM). This VDM would provide a standard for representing a more detailed abstract of the IC without exposing any of the IC’s intellectual property (IP). As an example, the VDM would contain information about what physical block, reference voltage, clock domain and drive strength associated to each I/O. This level of additional data would allow the package and board design teams the flexibility to optimize the signal interconnect throughout the system with very little impact on the IC’s performance. This VDM is the basis for a novel co-design methodology.

Leveraging the VDM, a more complete co-design methodology could be put in place. For optimal results, this co-design methodology should be adopted early in the IC floor-planning stage.
B. Next generation co-design methodology

There are several key ingredients to building a robust co-design solution. For starters, the design environment should be able to read/write data from all three design domains (IC, Package & PCB). Leveraging industry standard formats (Verilog, VHDL, GDSII, Excel, AIF, etc.) is considered for automating this task.

Another integral piece of a cross-domain methodology is connectivity management. This is required to capture and manage the system level connectivity; that is, the connectivity that spans across the IC, Package substrate and PCB. Since a signal name often changes between domains, automated pin mapping is required. Since recent trends for capturing connectivity for large IC’s have focused on tables, large interconnect tables should be supported, as well as traditional graphic based schematics. This should be a single design tool that supports a combination of both methodologies to support mixed signal designs.

Often overlooked by the chip (and package design) team is the generation of the schematic symbol that is critical to the PCB design process. These symbols will often have hundreds or even thousands of pins. The signal assignments to these pins have the potential to change frequently in the co-design process. Not providing an automated solution for this process would introduce the potential for human error into the co-design flow. Therefore, a complete co-design methodology must automate these updates. This process would provide the user the ability to divide the device into multiple symbols as required for fitting on the appropriate schematic sheet while adhering to company graphic standards.

Along with the connectivity that traverses across these design domains are the design constraints. These would include local (specific to a single domain) as well as system level (cross domain) rules. Defining and managing these constraints would need to be tightly linked with connectivity management tool.

Generation of the physical devices in a co-design flow is equally important. Before any physical I/O and interconnect can be optimized, models must be available for the IC, package and PCB footprints. The IC footprint data would be included in the VDM and automation of this footprint is straight forward. However, physical footprint data is also required for the package and the various PCB level devices that will be used for optimization. In addition to the physical pin locations, it is important to include the break-out and fan-out routing for these devices. This data is critical for higher pin count devices and should not be overlooked. Connectivity from the IC pad all the way through to the final PCB route destination is the ideal data set for I/O optimization.

Fortunately, most physical library data can be automatically generated by simple software algorithms based on user entered parametric data or by reading existing spreadsheet part data. In addition, the ability to use the PCB design library for accurate board level physical devices is important. In some cases, during early planning, abstract data could be used to represent the physical device when not readily available from a given design team. This capability is particularly useful for prototyping and feasibility studies. The ability to generate this data quickly and easily is important to a successful co-design methodology.

Once the data is captured, all three design teams would be able to view, in a single graphical environment, the complete interconnect path from on-chip I/O to flip-chip bump, to package pin and finally to PCB level pin displayed as a flight line. This ability to visualize the complete interconnect path across the system is the basis for robust interconnect planning. It also gives an early indication of the routing challenges on the PCB and package substrate leading to more accurate schedule and cost planning for the complete system.

The basis for I/O and interconnect optimization begins here. This is the process of un-raveling the rats nest of flight lines across all three design domains. The random un-raveling of interconnect across the system is not realistic. Multiple pin/signal/bus rules need to be applied at the IC, Package and PCB levels. An advanced rule development capability that provides a straightforward way to constrain signals would support this. One example of this would be to set a pin adjacency rule for the positive and negative signals in a differential pair. Without a rule based methodology for the un-raveling process the design teams would be required to lock down most of the signals in their design. This would greatly reduce the effectiveness of any co-design methodology.
With the rules established, the optimization process would begin. The unraveling process could be run on entire signal paths across IC, Package and PCB. For detailed optimization, the user would focus on a section of the interconnect path at a time. The unraveling algorithm supports a reduction in length or a reduction in flight line cross-overs (layer reduction). This unraveling algorithm is the core of the methodology and once all of the data is available, it would likely be the most frequently used feature in the flow allowing layout specialists from each design domain the ability to quickly look at trade-offs between the IC, package and PCB layouts.

This paper recommends starting with the PCB level devices and optimizing inward to the package and then to the IC. This approach has been shown to greatly reduce the cost and design cycles for the complete system. And, with an accurate VDM in place, no significant impact on the IC would occur. The example shown uses a 3rd party DDR2 SDRAM device and PCI-Express connector to drive the optimization process from the board back up through the package onto the IC. The end result is a more routable PCB and package substrate with fewer layers (less cost).

During these early planning stages is also the best time to start to look at system level timing and potential Signal Integrity issues. Pre-route analysis could be performed by representing interconnect as estimated transmission lines, and simple lumped equivalent circuits. The results from any analysis run at this stage could be used to define constraints that would be used to drive the routing on the package substrate and PCB during final implementation.

This is also the ideal time to start to plan and analyze the power delivery network (PDN) across the PCB, Package and onto the IC. Integration with an accurate Power Integrity (PI) tool could prove invaluable. Early analysis data could be used to drive the correct signal to power ratio for the flip-chip bump array mentioned above. It could also be used to make trade-offs between on-package and PCB level decoupling.

### III. SUMMARY

The overall cost of getting a chip ship in volume is a concern for many companies in today’s market. Industry leading companies are starting to implement co-design flows in hopes of reducing overall design cycles and cost. This paper proposes a novel approach to developing a co-design flow that is based on a new intelligent die abstract model (VDM) and a board driven methodology. This methodology has been used to save over 25% on a high volume production PCB.