Recent Research Development in PCB Layout

Tan Yan[†‡] and Martin D. F. Wong[‡]

[†]Synopsys, Inc., Mountain View, CA 94043, USA
[‡]Department of ECE, University of Illinois at Urbana-Champaign, Urbana, IL 61801, USA
Email: tanyan@synopsys.com, mdfwong@illinois.edu

***Abstract*—The increasing complexity of electronic systems has made PCB layout a difficult problem. A large amount of research efforts are dedicated to the study of this problem. In this paper, we provide an overview of recent research results on the PCB layout problem. We focus on the escape routing problem and the length-matching routing problem, which are the two most important problems in PCB layout. Other relevant works are also briefly introduced.**

I. Introduction

The constantly evolving manufacturing technology continues to push the complexity of integrated circuits to new heights. For example, the new Intel Core i7 contains more than 1 billion transistors. A direct result of this exploding complexity is the dramatic increase in the complexities of packages and printed circuit boards (PCBs). By the end of 2010, the pin count of high-end packages is expected to be around 4000 [1]. A typical high-end PCB could have more than 10 thousand signal nets. On the other hand, the size of a package is kept minimum. A dense packages could have a pin count of over 2000 while its size is only $47.5 \times 47.5\text{mm}^2$ [2]. This makes the footprint of such a package on PCB a very dense pin grid.

Such a large net count and high pin density make manual design of PCBs an extremely time consuming and error-prone task. Furthermore, the increasing clock frequency imposes special physical constraints such as length-matching routing, pairwise routing, planar routing, etc., on high-performance PCBs [3]–[6]. These constraints make traditional IC and PCB routers not applicable to modern PCB routing. To the best of our knowledge, there is no mature commercial automated router that handles these constraints well. Therefore, automated PCB routers that are tuned to handle such constraints is in great demand for modern high-performance PCB layout.

Because of such demand, a tremendous amount of research works are focused on PCB routing problems in recent years. Two major topics on PCB routing are escape routing and length-matching routing. In this paper, we give an overview of recent research efforts on these two topics.

The rest of this paper is organized as follows: Section II gives some background knowledge about the PCB routing problem. Then recent research advances on escape routing and length-matching routing are introduced in Section III and Section IV respectively. In the end, we briefly cover the research results in some other topics.

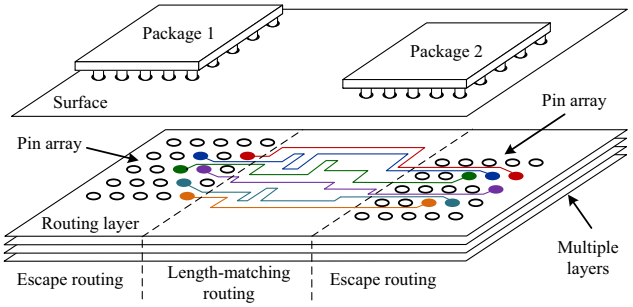

Fig. 1. An illustration of PCB routing.

II. PCB Routing Problem

A modern PCB usually hosts several chip packages whose footprints are arrays of pins (see Figure 1). Such pin arrays are expected to be connected by non-crossing wires. Not all connections can be routed on one layer, so multiple layers are used to accommodate all the wire connections. However, introducing vias at the middle of a route would introduce reflection and ringing effects which can cause serious signal integrity issues [5], [6]. Therefore, it is highly preferred that no vias are inserted in the middle of the routing (vias are allowed at the two ends to connect to the package pin/ball). This requires the routing of a signal net to be planar without switching layers in the middle. This planar routing style makes PCB routing very different from IC routing, which uses conventional XY routing style with a preferred routing direction for each routing layer. Therefore, conventional IC routing algorithms cannot be used to solve the PCB routing problem.

There are two important problems in PCB routing:

1) **Escape routing problem**: route from pins inside the pin arrays to the boundary of the arrays (help the pins "escape" the pin array).
2) **Length-matching routing problem**: connect the escaped routes between the pin arrays while satisfying stringent length constraints.

Escape routing and length-matching routing have different tasks. Since escape routing usually dominates the total number of layers, its major task is to escape a set of pins using as few layers as possible. Sometimes it may also need to provide a matching net orderings along the boundaries of the two arrays in order to provide a planar topology for later length-matching routing. The focus of length-matching routing, on the

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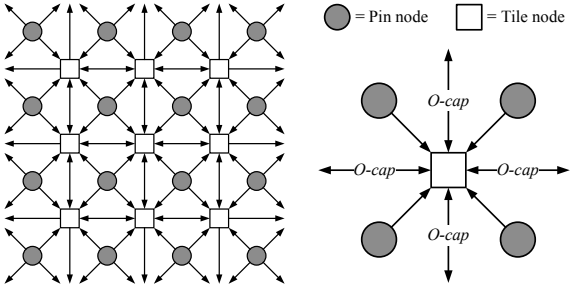

(a) Flow model for a pin grid (b) Inside a tile

Fig. 2. Typical network-flow model for unordered escape routing problem.

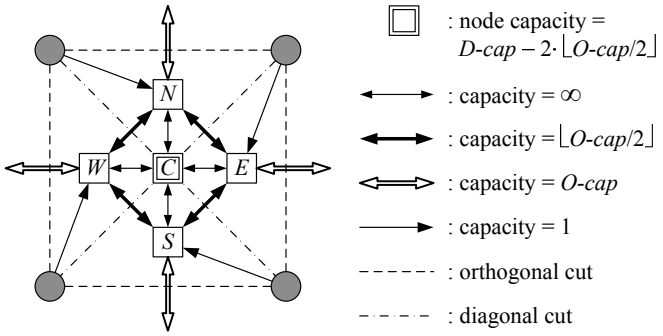

Fig. 3. Yan and Wong's [12] network-flow model inside a tile.

other hand, is to carefully detour the wires to meet the length constraints while maintaining the planar topology inherited from escape routing.

III. Escape Routing

Among all the PCB routing problems, escape routing is probably the most intensively studied problem. It is to route from specified pins in a pin array to the boundary of the array. It can be further classified into three categories:

- **Unordered escape** is to route from the pins inside a pin array to the boundary of the array without any constraint on the pin ordering along the boundary.
- **Ordered escape** also considers only one pin array. However, it requires the escape routing to conform to a specified ordering along the boundary.
- **Simultaneous escape** considers escape routing of two pin arrays. The ordering of the escaped routes in the two arrays are required to match in order to provide a planar topology for later length-matching routing.

The three types of escape routing problems all have applications in PCB routing.

Both unordered and ordered escape routing problems involve only a single pin array. Studies of these problems are initiated not only from PCB routing researches but also package routing researches because in package design, people also face the problem of routing from inside a pin array to some linearly arranged bonding pads. Simultaneous escape routing, however, is only for PCB routing.

A. Unordered Escape

Network-flow approaches are pervasively used to solve the unordered escape routing problem. The idea is to view each routing path as a unit flow from the pin to the boundary. Since no ordering is specified, a flow solution always corresponds to some non-crossing routing. A typical network model looks like Figure 2. Representative works using network-flow to solve the unordered problem include Fang et al.'s works on flip-chip design [7]–[9] and Yu et al.'s work on package routing [10]. Note that Yu et al.'s work is not completely based on the network model in Figure 2. Their network is based on triangulation of the pins because they do not assume a regular rectangular grid structure of the pins. In Wang et al.'s work on layer minimization [11], network-flow is used to analyze the problem and estimate the maximum number of escapable pins.

The model in Figure 2 works well if we only consider orthogonal wiring capacity, which is the maximum number of wires allowed between two horizontally or vertically adjacent pins. It does not capture the diagonal capacity because the number of wires passing between two diagonally adjacent pins cannot be correctly captured by this model. Yan and Wong [12] proposed a network model that could correctly capture the diagonal capacity as well as orthogonal capacity. By adding nodes and edges, they are able to control the flow in finer detail inside each tile and thereby capture the diagonal capacity. Their network model is illustrated in Figure 3. Their other contribution is to consider missing pins in their model.

There are also non-flow solutions to the unordered escape routing problem. For example, Yu and Dai [13], [14] used monotonic routing style to escape all the pins in a pin grid on one layer. However, non-flow solutions are usually used to solve full grid escape problem, which means all the pins in the grid are expected to be escaped in one or multiple layers, which is a common problem for package routing. In PCB routing, we often face the problem when a set of specified pins are expected to be escaped on the same layer. In that case, network-flow is still the most popular approach.

B. Ordered Escape

For ordered escape problem, network-flow does not work because flow does not carry the ordering information. Researchers usually rely on either heuristics that may lose optimality or exponential time approaches such as Integer Linear Programming (ILP) or Boolean Satisfiability (SAT) solver.

In [15], Fang et al. formulated the ordered escape routing problem as an ILP problem and use an ILP solver to solve the problem optimally. With their reduction technique, they were able to prune the number of variables by 99.9%. Such a variable reduction is very useful because it brings down the run time for a fairly large design (over 1000 pins) down to about an hour, which is acceptable considering human designers will spend much more time routing it manually. Unfortunately, since they consider non-monotonic routing only when their routing graph has a cycle, their ILP formulation does not guarantee optimality.

In [16], Luo and Wong proposed to transform the ordered routing problem into Boolean Satisfiability (SAT) problem and use SAT solver to solve the problem. Their formulation does not have any assumption on the routing style, meaning that their approach can guarantee to find a solution if there exists one. It is the first work that can optimally solve the ordered escape routing problem. However, this optimality comes at a price. It would take the router about 10 minutes to route a 10×10 grid and the time complexity grows very fast when the grid size increases. However, they also proposed a partition technique to decompose a large problem into smaller problems. By doing that, the runtime could be significantly cut down. In a later paper [17], Luo and Wong extended their router to handle cyclic ordering and pin clustering. Because their router is very powerful in solving small but difficult problems, they also propose to use their router to rip-up and reroute a small region where other heuristic-based routers fail to complete the routing.

Another route that researchers took to tackle the problem is to simplify the problem by adding constraints on the routing. The most popular constraint used is the monotonic routing constraint. The escape routing of a pin is called *monotonic* if it goes to the target pin grid boundary without turning back. Kubo and Takahashi's work [18], [19] on two layer escape routing and via assignment for packages adopts this monotonic routing style. In their work, they assume that the escape routing follows monotonic style and perturb the via assignment iteratively to search for suitable via assignment and escape routing. This approach was then enhanced by Tomioka and Takahashi [20] to achieve better routability.

In another paper by Tomioka and Takahashi [21], they studied the cases where pins are escaped through a corner of a pin grid or through the opposite two sides of a pin grid. They discovered the necessary and sufficient conditions for planar topological solutions to exist in those two cases. They also proposed an routing algorithm based on the discovered necessary and sufficient conditions.

The work by Lee et al. [22] does not put monotonic constraint on the routing. Their routing algorithm is based on computing the *weighted longest common subsequence* and *maximum planar subset of chords*. They compared their router with the ILP-based router in [15] and showed a 122x speedup.

C. Simultaneous Escape

Different from the single component escape routing problems which are common for both package and PCB routing, simultaneous escape routing problem is unique to PCB routing. Therefore, there are less research works under this category.

The earliest work on this problem is Ozdal and Wong's work [23], [24]. Their idea was to first generate a few simple routing patterns for each pin and then choose one routing pattern per pin such that the mismatched net ordering along the two boundaries is minimized. They intelligently modeled the pattern selection problem as a *longest path with forbidden pairs* problem and proposed an exact polynomial-time algorithm that is guaranteed to find the maximal planar routing solution on one layer. For large problems, they proposed a randomized algorithm that has better scalability. In a later paper [25], they presented several enhancements on this router: 1) they used a congestion-driven router to generate the routing patterns and 2) they took performance constraints into consideration. The effectiveness of their approach is largely determined by the routing patterns generated in the first step. The router performs well when good routing solutions can be captured by the generated patterns. Unfortunately, the shape of the escape routing can be very complicated in difficult escape problems. In this case, it can be very tricky to predict what patterns should be generated to capture a good solution.

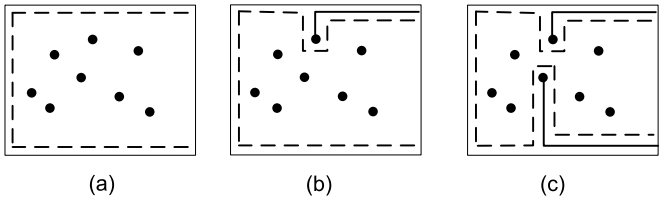

Fig. 4. An illustration of boundary routing [26].

In [26], Luo et al. presented a novel *boundary routing* approach to solve the simultaneous escape routing problem. Essentially, their idea is to build a routing boundary for all the pins inside a pin grid and let the routing path follow the boundary as much as possible when routing a net. After a net is routed, the routing boundary is shrunk to exclude the routed net. Figure 4 illustrates this idea. Although their strategy looks very simple, experiments show that this strategy is very effective in solving difficult problems. For a set of industrial escape problems, their router successfully solved all of them while Cadence Allegro PCB router was only able to complete the routing for half of the problems. Figure 5 shows their routing result for one problem.

One interesting work worth mentioning is the *potential router* proposed by Kajitani [27]. The idea is based on the analogy between planar routing and equipotential lines in an electric field. Equipotential lines are naturally planar. Therefore, we can view any planar routing as the equipotential lines in certain electric field. On the other hand, by enumerating possible configurations of the electric field, one could enumerate possible planar topologies for the routing. Since this work focus on planar topology in general, its theory can be applied to all three types of escape routing problems.

IV. Length-Matching Routing

Length-matching routing is to connect the escaped routes between the boundaries of pin arrays while satisfying certain length constraints. Due to the high clock frequencies on today's high-performance boards, the nets are usually subject to very stringent length constraints. There are two types of length-matching constraints:

1) **Min-max length bounds**: each net is given minimum and maximum length bounds and the length of the routing must be within the bounds.

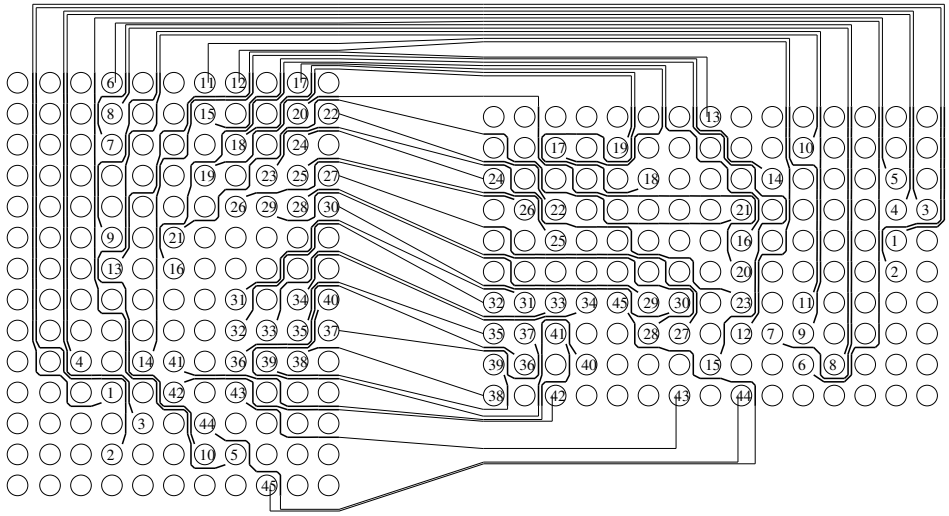

Fig. 5. Simultaneous escape routing solution produced by Luo et al.'s router [26].

2) **Bounded length difference**: a group of nets are expected to have similar length. In other words, the difference between the lengths of a group of nets must be limited by some given bound.

In order to meet the minimum length bound or to minimize the length difference, we may need to lengthen wires that are too short. This make the length-matching problem unique because intentionally increasing the wire length is usually discouraged in many other routing problems.

A common way to increase the wire length is to snake the wire. However, snaking one wire generates a large blockage for other wires. In order to avoid this blockage, other wires may need to be detoured, potentially causing their maximum length bounds to be violated. As a result, greedy approaches would usually fail because they lack the global view of balancing the needs of all the wires. How to carefully distribute the limited routing resources so that the length requirements of all the nets can be satisfied is the key to this problem.

The first work that does non-greedy resource allocation for wire extension is by Ozdal and Wong [28], [29]. They used a Lagrangian relaxation based routing scheme to control the length of each net. In their routing scheme, Lagrangian multipliers are iteratively updated to reflect the current resource need of each net. A special router is called in each iteration to route the nets according to the resource need implied by the multiplier. In general, their approach provides good results. However, it has two potential issues:

- A router must be called *iteratively* to perform the actual routing. When the problem is large and difficult, it needs many iterations to converge to a solution, resulting in very long runtime.
- The routing of each net must be monotonic in one direction. This limits the possible topology of the solution and therefore limits the application of this approach.

In a later work, Ozdal and Wong [30], [31] proposed an algorithm for length-matching routing inside a channel. They first used river routing to derive the routing boundary of each net and then detoured each net inside its bounded area. They showed that their algorithm can approximate the optimal solution by a constant factor. This approach can achieve quite significant speedup compared to the Lagrangian relaxation based approach because it avoids calling a router iteratively. However, since only channel routing problem is considered, this approach has even more limited applications.

Length-matching routing inside a channel is also challenged by Kubo et al. [32]. They used a *symmetric-slant grid interconnect* scheme to reduce the length-matching problem into a general grid routing problem. The advantage of their work is that it can also handle multi-sink nets. However, their approach is for IC routing and therefore assumes a XY routing style, which is not practical for PCB routing.

Recently, Yan and Wong [33] proposed a length-matching algorithm that does not impose any restriction on the routing topology. Neither does their router require the pins to be aligned along a channel nor does it limit the routing to be monotonic. Their key idea was to view the length-matching routing problem as an area assignment problem and use a placement structure, Bounded-Sliceline Grid (BSG) [34] to help transform the area assignment problem into a mathematical programming problem. An iterative approach was then used to solve this mathematical programming problem. Besides capable of handling general topology, another big advantage of this router is that it is gridless. Unlike all previous routers, its performance does not depend on the routing grid size. This feature leads to very good scalability and is extremely useful because modern PCB routing configurations usually imply huge routing grids. This advantage was verified by their experiments. In one of their data, they achieved a 1000x speed up over the Lagrangian relaxation based router in [29]. Their router is very effective in solving difficult problems. Figure 6 illustrates one of their routing result. It can be seen that their router could efficiently utilize

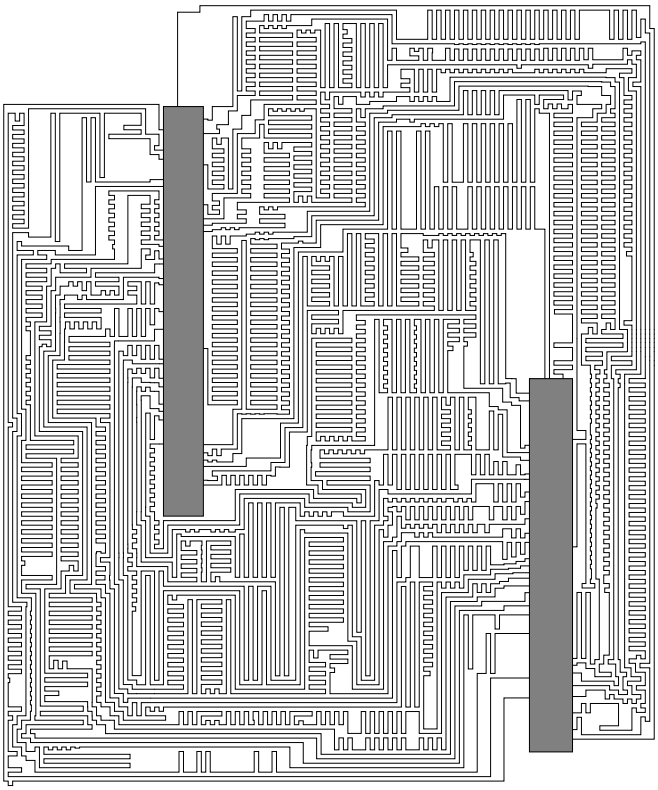

Fig. 6. The routing result of Yan and Wong's [33] length-matching router.

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the routing space for wire extension. In a later paper [35], they extended their router to handle multi-layer routing and multiple separation rules. However, one potential drawback of their work is that their routing scheme assumes a given topology. Such a topology is easy to generate if there are not many obstacles. However, if the design is filled with many obstacles, then generating a good topology for their router could be non-trivial.

Yan and Wong [36], [37] also proposed a preprocessing step to untangle the twisted nets for length-matching routing. They proposed a single-detour routing style and did a series of theoretical studies on this style. Their work was then followed up by Yan and Chen [38], who considered untangling on both ends of the routing.

V. Other Works

There are many other works on PCB layout that do not fall into the previous two categories. In this section, we do a very brief overview of the related works.

Works in previous two sections consider the PCB routing problems on net level. Hui et al. published a series of papers studying PCB routing problems on bus level [39]–[42]. In these works, they adopt a *projection based* escape routing style. The escape routing of each bus is bounded by a rectangle formed by projecting the pin cluster of the bus toward the boundary of the pin grid (see Figure 7). In [42], they compared their projection based pin assignment

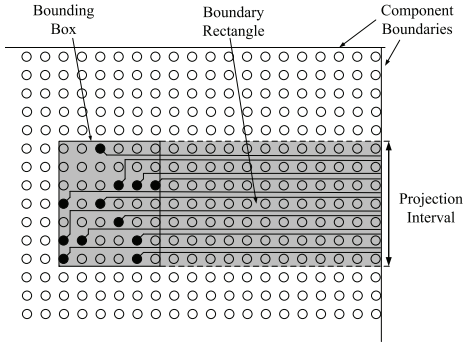

Fig. 7. Projection based escape routing

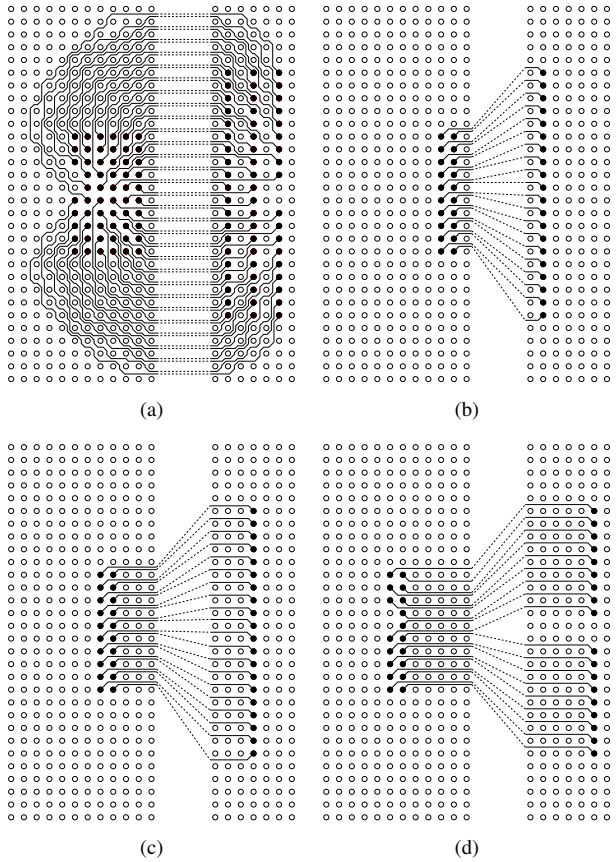

Fig. 8. Single-layer escape vs. projection based multi-layer escape. (a): single-layer escape routing; (b), (c), (d): projection based 3-layer escape routing.

and escape routing solution with single-layer escape routing solution and claimed that the projection based multi-layer solution usually results in shorter wire length and occupies smaller routing space. Figure 8 illustrates this argument. It can be seen that the multi-layer routing solution produced by their projection based scheme has shorter and straighter wires. Moreover, if we escape all the pins in one layer, we will obtain very imbalanced wire length: some pins have very long detours in their escape routing while some other pins escape without any detour. This dramatic difference in wire

lengths makes later length-matching routing a much more challenging problem. On the other hand, the projection based multi-layer solution has very straight wires. Therefore, the length difference is much smaller, making length-matching routing an easier problem.

In another work [39], Hui et al. proposed an optimal algorithm to select a maximum subset of buses such that their projection rectangles do not have any conflict. Yan et al. [43] then proposed an algorithm to solve the multi-layer bus assignment problem. The algorithm can optimally assign all the buses to multiple layers while keeping the total number of layers at minimum. In [40], Kong et al. studied the problem where buses are projected toward all four sides of a pin grid and proposed an optimal algorithm to find a maximum non-conflicting subset of the buses.

Global planning of buses are studied by Kong et al. in [41]. They proposed the first automatic bus planner for PCB routing. Their bus planner not only performs global routing of buses on each layer, but also does layer assignment. They tested their planner on a state-of-the-art industrial board (7000+ nets and 12 layers) and achieved very good routability. Length constraints were also considered in their work.

Pin assignment problem for PCB is studied in [44]. In the paper, Meister et al. proposed four heuristics for pin assignment considering both wire length and routability. Since escape routing is not performed, their approach may run faster than the simultaneous pin assignment and escape routing scheme in [42] although no comparison is made in the literature.

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