Low-power Clock Trees for CPUs

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Abstract—Clock networks contribute a significant fraction of
dynamic power and can be a limiting factor in high-performance
CPUs and SoCs. The need for multi-objective optimization over a
large parameter space and the increasing impact of process vari-
ation make clock network synthesis particularly challenging. In
this work, we develop new modeling techniques and algorithms,
as well as a methodology, for clock power optimization subject to
tight skew constraints in the presence of process variations. Key
contributions include a new time-budgeting step for clock-tree
tuning, accurate optimizations that satisfy budgets, modeling and
optimization of variational skew. Our implementation, Contango
2.0, outperforms the winners of the ISPD 2010 clock-network
synthesis contest on 45nm benchmarks from Intel and IBM.

I. INTRODUCTION

Processor-based systems fueled the development of elec-
tronics since the 1960s. PCs were the main driver of growth
in electronics in the 1990s, and in the 2000s mobile phones and
other battery-powered consumer devices became a significant
market segment, followed by automotive electronics. The
emphasis in CPU design has shifted from high performance
to power-performance-cost trade-offs, including the advent of
multicore CPUs and the growing popularity of low-power
ARM CPUs. In the netbook market, the low-power 1.6GHz
Atom CPU from Intel is currently competing with ARM’s
multicore 2GHz Cortex-A9 CPUs and the 1GHz Cortex-
A8, but 98% of world’s mobile phones rely on ARM-based
CPUs [13] which currently offer better power-performance-
cost trade-offs than Intel CPUs [24].

ARM cores often drive system-on-chip (SoC) designs, laid
out using low-power ASIC methodologies. Such methodologies
perform automated clock-tree synthesis after placement,
whereas traditional high-performance CPU methodologies pre-
design clock networks and use active deskewing to lower clock
skew and susceptibility to process variations [19]. Clock trees
are more susceptible to variations than meshes (common in
CPUs), but are 2-4 times more power-efficient. This is signif-
ificant because clock distribution networks and corresponding
sequential elements consume up to 70% of CPU power and can
affect power-performance comparisons between CPUs [20].

Recent developments in embedded CPU design stress the
need for low-power clock trees, yet also impose stringent
skew limits, especially in the presence of process, voltage and
temperature (PVT) variation for sub-45nm CMOS technology.
Previous clock-tree methodologies rely on symmetric and reg-
ular tree topologies, such as H-trees and fishbones [1, chapter
43], which do not require sophisticated design algorithms (see
Section II). However, these topologies experience difficulties
with layout obstacles, non-uniform sink distributions, and
varied sink capacitances. Fully-automated clock-tree synthesis
supported by commercial EDA tools offers clear advantages in
terms of capacitance, but may not be able to ensure sufficiently
low skew for use in a 2GHz CPU. For example, the authors of
[17] report clock trees generated by Cadence tools with skew
that is orders of magnitude higher than the single-ps skew
provided by clock meshes.

In this paper, we pursue the following research questions.
• How far can the skew of a high-performance clock tree
be optimized?
• How can one minimize the impact of PVT variations in
a clock tree?
• Given a single-picosecond skew requirement, how com-
petitive are clock trees with clock meshes?

Our approach to answering these questions is inspired by the
ISPD 2010 clock-network synthesis contest, which used sev-
eral 2GHz CPU benchmarks from IBM and Intel to compare
tools submitted by 10 teams across the world (downselected
from 20 initial registrants). To evaluate the quality of the clock
networks, difficult slew and skew constraints were checked
against 45nm Monte-Carlo SPICE simulations that modeled
PVT variations. Clock networks that cleared all constraints
were compared by their total capacitance — a proxy for
dynamic power. In this context, we developed a suite of algo-
rithms for the design and thorough optimization of clock trees.

The results of the ISPD 2010 contest offer a rare opportunity
to compare multiple strategies for clock-network synthesis —
the third-place team used symmetric trees [23], the second-
place team used clock meshes, and our team won the contest
by optimizing clock trees built by the DME algorithm [2], [6].

Specific innovations in our comprehensive methodology for
clock-network synthesis include
• The notion of local-skew slack for clock trees.
• A tabular technique to estimate the impact of variations
on skew between two sinks.
• A path-based technique to enhance the robustness of a
clock tree to PVT variations.
• A time-budgeting algorithm for clock-tree tuning that
distributes delay targets to individual edges of the tree so
as to improve skew with minimal power resources. This
algorithm can be used in the context of PVT variations
and is not specific to our methodology.
• Fine tuning of optimized clock trees by gentle wire
snaking, sufficiently accurate to satisfy delay budgets.

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Our empirical results are compared to those of the winners of the ISPD 2010 clock-network contest, where each team violated prescribed skew constraints (7.5 ps in most cases) on at least some benchmarks in the presence of variations. However, results reported in this paper satisfy skew constraints on every benchmark. Our experimental results have recently been developed for the ISPD 2009 clock-network synthesis contest which focused on ASIC and SoC designs. A clock-synthesis methodology for SPICE-accurate skew optimization with tolerance to voltage variations called Contango was proposed in [14]. Dynamic Nearest-Neighbor Algorithm to generate tree topology and Walk-Segment Breadth First Search for routing and buffering were proposed in [22]. A three-stage CLR-driven CTS flow based on an obstacle-avoiding balanced clock-tree routing algorithm, monotonic buffer insertion, as well as wire-sizing and wire-snaking is proposed in [15].

Several methodologies for clock-tree tuning have recently been developed for the ISPD 2010 clock-network synthesis contest which focused on ASIC and SoC designs. A clock-synthesis methodology for SPICE-accurate skew optimization with tolerance to voltage variations called Contango was proposed in [14]. Dynamic Nearest-Neighbor Algorithm to generate tree topology and Walk-Segment Breadth First Search for routing and buffering were proposed in [22]. A three-stage CLR-driven CTS flow based on an obstacle-avoiding balanced clock-tree routing algorithm, monotonic buffer insertion, as well as wire-sizing and wire-snaking is proposed in [15].

A. Global and local skew

Common terminology and notation are introduced next. Definition 1: Given a clock tree $\Psi$, let $\lambda(s_i)$ be the clock latency (insertion delay) at sink $s_i \in \Psi$. Then the skew between two sinks $s_i$ and $s_j \in \Psi$ is defined as

$$\text{skew}^\Psi(s_i, s_j) = |(\lambda(s_i) - \lambda(s_j))|$$

(1)

Global skew is defined as

$$\omega^\Psi = \max_{s_i, s_j \in \Psi} \text{skew}^\Psi(s_i, s_j) = \max_{i \in \Psi} \lambda(s_i) - \min_{i \in \Psi} \lambda(s_i)$$

(2)

Nominal values of skew $^\Psi(s_i, s_j)$ and $\omega^\Psi$ are computed neglecting the impact of variations. Global skew can be improved by decreasing $\max_{i \in \Psi} \lambda(s_i)$ (speeding up the slowest sinks) or increasing $\min_{i \in \Psi} \lambda(s_i)$ (delaying the fastest sinks).

Table II

<table>
<thead>
<tr>
<th>ISPD 10 Bench.</th>
<th>Provider</th>
<th>Area, $\mu m^2$</th>
<th>Num. sinks</th>
<th>Obstacles, $\mu m$</th>
<th>$\Delta_s$</th>
<th>$\Omega_{\Delta_s}$</th>
</tr>
</thead>
<tbody>
<tr>
<td>CNS01</td>
<td>IBM</td>
<td>64</td>
<td>1107</td>
<td>4</td>
<td>600</td>
<td>7.5</td>
</tr>
<tr>
<td>CNS02</td>
<td>IBM</td>
<td>91</td>
<td>2249</td>
<td>1</td>
<td>600</td>
<td>7.5</td>
</tr>
<tr>
<td>CNS03</td>
<td>IBM</td>
<td>1.51</td>
<td>1200</td>
<td>2</td>
<td>370</td>
<td>4.999</td>
</tr>
<tr>
<td>CNS04</td>
<td>IBM</td>
<td>5.73</td>
<td>1845</td>
<td>2</td>
<td>600</td>
<td>7.5</td>
</tr>
<tr>
<td>CNS05</td>
<td>IBM</td>
<td>5.9</td>
<td>1016</td>
<td>1</td>
<td>600</td>
<td>7.5</td>
</tr>
<tr>
<td>CNS06</td>
<td>Intel</td>
<td>1.74</td>
<td>981</td>
<td>0</td>
<td>600</td>
<td>7.5</td>
</tr>
<tr>
<td>CNS07</td>
<td>Intel</td>
<td>3.67</td>
<td>1915</td>
<td>0</td>
<td>600</td>
<td>7.5</td>
</tr>
<tr>
<td>CNS08</td>
<td>Intel</td>
<td>2.99</td>
<td>1134</td>
<td>0</td>
<td>600</td>
<td>7.5</td>
</tr>
</tbody>
</table>

TABLE II

ISPD 2010 benchmarks based on 45 nm Microprocessor Designs. $\Omega_{\Delta_s}$ is the local skew limit, and $\Delta_s$ is the local skew distance limit respectively (see Section III-A). Nominal voltage is 1.0V and on-chip variations ($\nu$) are accounted by 15% voltage variation and 10% variation of wire parasitics for all benchmarks [25].
between adjacent and connected sinks is a more meaningful optimization objective [8], [18]. Local skew is defined by restricting eligible sink pairs to be within distance $\Delta > 0$, which is determined for a given circuit after timing-driven placement.

Definition 2: Given a clock tree $\Psi$ and a local skew distance bound $\Delta > 0$, let $\text{dist}(s_i, s_j)$ be the Manhattan distance between sinks $s_i$ and $s_j \in \Psi$. Then the worst local skew [25] is defined as

$$\omega^\Psi = \max_{\text{dist}(s_i, s_j) < \Delta} \text{skew}^\Psi(s_i, s_j)$$  \hspace{1cm} (3)

Reducing skew down to single picoseconds in the presence of variations may require a significant increase in power consumption. Since more than 30% of total power in modern microprocessors is consumed by clock networks, minimizing clock-network capacitance is as important as skew minimization. Therefore modern circuit designs can tolerate a certain amount of clock skew, and power can be reduced provided that the clock network remains below a given skew bound, even in the presence of variations.

Definition 3: Consider a clock tree $\Psi$, a local skew distance bound $\Delta > 0$, variation model $\nu$ and target yield $0 \leq y \leq 1$. Let $\Psi_\nu$ be the clock tree $\Psi$ with variation $\nu$ and $f(t)$ be the cumulative distribution function of $\omega_\nu^\Psi$. Then the worst local skew with variation is defined as

$$\omega^\Psi_{\nu, y} = f^{-1}(y)$$ \hspace{1cm} (4)

Viewing the local skew limit $\Omega_\Delta$ as a design constraint (see Table II), we pursue the following goals.

1) Building variation-tolerant clock networks with $\omega^\Psi_{\nu, y} < \Omega_\Delta$, subject to slack constraints.
2) Minimizing clock-tree power.

B. Local-skew slack

Given a clock tree with known sink latencies, one can optimize it using delay budgets derived from the sink- and edge-skew calculation [14, Section 3], followed by global skew optimization to reduce global skew below $\Omega_\Delta$. This strategy is sound because local skew $\omega_\Delta$ cannot exceed global skew. However, global skew optimizations attempt to reduce skew between sinks more distant than $\Delta$, which may require unnecessary increase in power.

To tune the clock tree on a tight power budget, we propose the concept of local-skew slack.

Definition 4: Given a clock tree $\Psi$ and local-skew constraints $\Omega_\Delta$, the local-skew slack $\sigma(s)$ for a sink $s \in \Psi$ is the minimum amount of additional delay in picoseconds for $s$, so that the tree satisfies $\omega^\Psi_{\nu, y} < \Omega_\Delta$.

The $\Delta$-neighborhood of sink $s_i$ is $\mathcal{N}(s_i) = \{ s \in \Psi \mid \text{dist}(s, s_i) < \Delta \}$. It is used in Algorithm 1 to calculate $\sigma(s)$ for every sink. This algorithm uses $\text{varEst}(s_i, s_j) = 0$ in the absence of variations, and otherwise the definition in Section III-C.

Once local-skew slacks $\sigma(s)$ are computed for all sinks, we define local-skew slack of tree edge $e$ as the smallest slack of a downstream sink. Edge slacks in the entire tree can be computed by one recursive tree traversal in linear time, giving the optimal amount of tuning to improve worst local skew [14, Section 3]. Figure 1 illustrates the computation of local-skew slack for sinks and edges.

C. Modeling process variation

Designing low-capacitance low-skew clock trees without considering process, voltage and temperature variations often results in significant skew in each chip. However, variation-aware optimization has not been explored until recently and requires reliable estimation techniques. Monte-Carlo simulations are slow and not suitable to clock network optimization. Instead, we develop a tabular technique to account for variation in single-shot timing analysis.

When two sinks can be connected by a short path in the tree, variation of skew between them is small. On the other hand, variational skew between sinks that are geometrically close can be significant if the unique tree-path between them is long. This is illustrated in Figure 2.

Our key insight is that the impact of variations on skew between two sinks is closely correlated with tree path length and how the tree path is buffered. Therefore, for a given technology node, buffer library, wires and variation model, we propose to build a look-up table with comprehensive information regarding the worst-case variation on skew for various paths between pairs of sinks.
Algorithm 1 Computing local-skew slack for sinks

\[ \sigma = 0; \]\text{ //Set of minimum local slack}\\
\( \text{SinkQ} = \emptyset; \) \text{ //Sinks to be optimized}\\
\textbf{for each} sink \( s_i \) \textbf{ do}\\
\quad \textbf{for each} \( s_j \) in \( N(s_i) \) \textbf{ do}\\
\quad \quad \text{if} (\lambda(s_i) + \lambda(s_j) \text{ and}\\
\quad \quad \text{skew}(s_i, s_j) + \text{varEst}(s_i, s_j) > \Omega_\Delta) \text{ then}\\
\quad \quad \quad \text{SinkQ.enqueue}(s_i);\\
\quad \quad \textbf{end if}\\
\quad \textbf{end for}\\
\textbf{end for}\\
\textbf{while} \text{size(SinkQ)} \neq 0 \textbf{ do}\\
\quad s_i = \text{SinkQ.dequeue}(); \text{MaxSlack}=0;\\
\quad \textbf{for each} \( s_j \) in \( N(s_i) \) \textbf{ do}\\
\quad \quad \text{if} \ (\text{MaxSlack} < \text{skew}(s_i, s_j) + \text{varEst}(s_i, s_j) - \Omega_\Delta)\\
\quad \quad \quad \text{then}\\
\quad \quad \quad \quad \text{MaxSlack} = \text{skew}(s_i, s_j) + \text{varEst}(s_i, s_j) - \Omega_\Delta;\\
\quad \quad \textbf{end if}\\
\quad \textbf{end for}\\
\quad \sigma_{s_i} = \text{MaxSlack};\\
\quad \textbf{for each} \( s_j \) in \( N_i \) \textbf{ do}\\
\quad \quad \text{if} \ (s_j \notin \text{SinkQ} \text{ and } \lambda(s_j) + \sigma_{s_j} < \lambda(s_i) + \sigma_{s_i} \text{ and}\\
\quad \quad \quad |(\lambda(s_j) + \sigma_{s_j} - (\lambda(s_i) + \sigma_{s_i})) + \text{varEst}(s_i, s_j) > \Omega_\Delta|)\\
\quad \quad \quad \text{then}\\
\quad \quad \quad \quad \text{SinkQ.enqueue}(s_j);\\
\quad \quad \textbf{end if}\\
\quad \textbf{end for}\\
\textbf{end while}\\

\begin{definition} \text{Given a technology node } T, \text{ buffer and wire library } B, \text{ variation model } \nu \text{ and desired yield } 0 < y \leq 1, \text{ let } \Xi_{T,B,\nu,y}[w,b,t] \text{ be the variation-estimation table which returns the worst-case increase in skew (with probability } y) \text{ between two sinks connected by a tree path of length } w \text{ with } b \text{ buffers and the buffer type } t. \text{ When multiple buffer types are used in the tree path, } t \text{ is the smallest type in the tree path, so as to avoid under-estimation of variation.} \end{definition}\\

\text{To build the table, we generated a large number of test trees on public CNS benchmarks and randomly generated benchmarks. The initial tree-construction method explained in Section IV with various buffer types is utilized for the test trees. The number of Monte-Carlo SPICE simulations is determined based on the given variation model } \nu. \text{ Variational skew between any two sinks during the simulations is recorded in the table with classification by } w, b \text{ and } t. \text{ The table is later restructured to represent a probability density function for each } (w, b, t) \text{ entry in order to look up with yield } y. \text{ Building the variation-estimation table requires extensive simulations, but once the table is built, it can be used for many clock trees. To determine the impact of variation on skew between sinks in a clock tree, a function } \text{varEst}(s_i, s_j) \text{ is defined as follows. Given a clock tree } \Psi \text{ and a variation table } \Xi_{T,B,\nu}, \text{ let } L(s_i, s_j) \text{ be the total length of wires, } b_n(s_i, s_j) \text{ be the total number of buffers and } b_l(s_i, s_j) \text{ be the largest buffer type in the tree path between two sinks } s_i \text{ and } s_j \in \Psi. \text{ The variation table is accessed by the function } \text{varEst}(s_i, s_j) = \Xi_{T,B,\nu} [L(s_i, s_j), b_n(s_i, s_j), b_l(s_i, s_j)].\end{definition}\\

\begin{align} \text{Theorem 1:} \quad & \omega^{\Psi}_{\nu,y} < \Omega_\Delta \text{ only if} \\
& \text{skew}(s_i, s_j) + \text{varEst}(s_i, s_j) < \Omega_\Delta \forall s_i, s_j \in \Psi \tag{5} \end{align}\\

\section{IV. Initial Tree Construction and Buffer Insertion}\\
\begin{figure}[h]\\
\centering\\
\subfloat[Nominal sink latencies]{{B(766ps)\ A(764ps)\ C(767ps)\ D(765ps)}}\hspace{1cm}\\
\subfloat[Latencies with variation]{{B(766ps)\ A(764ps)\ C(767ps)\ D(773ps)}}\\
\caption{The impact of variations on local skew. Sinks are indicated by crosses, the clock source is indicated by a solid triangle. Nominal skew of 3 ps is shown in (a). Full skew of 11 ps is shown in (b), where some tree edges are delayed (thick red) and some are sped up (dotted green) by random variations. Only sink A is within the local skew distance from sinks B, C and D.}\\
\end{figure}\\

\text{We invoke the unmodified ZST-DME algorithm [4], [10] and perform initial buffer insertion to minimize source-to-sink Elmore delay, rather than skew or capacitance [7], [21]. Elmore delay is too inaccurate for skew optimization, but our approach creates significant room for tuning the clock tree by delaying fast paths [14]. In the presence of layout obstacles, proper obstacle-handling is required to avoid violations due to obstacles. The ISPD 2010 benchmarks include obstacles over which wire-routing is possible but buffer insertion is not allowed. We adapted a simple and robust technique for obstacle avoidance in clock trees from [14] which repairs obstacle violations in the trees obtained by the ZST-DME algorithm.}\\

\text{When multiple wire types are available, the choice of wires affects both total power and susceptibility to variations. Under tight skew constraints in high-performance CPU designs, thicker wires (on a given metal layer) are preferable because they limit the impact of variations and still allow for future power-performance trade-offs by wire sizing. In less aggressive ASIC and SoC designs, power optimization may motivate thinner wires. But upsizing wires in a reasonably tuned clock tree may be of limited use because it increases capacitance, potentially leading to slew violations.}\\

\text{Selecting buffer types for initial buffer insertion is also important. Given an initial tree without buffers } \Psi_0, \text{ let } t(s_i, s_j)
be the type of a buffer required for the tree path between two sinks $s_i$ and $s_j \in \Psi_0$ to satisfy $\text{varEst}(s_i, s_j) < \Omega_{\Delta}$. $t(s_i, s_j)$ can be found from the variation-estimation table $\Xi_{T, B, \nu}$ with $L(s_i, s_j)$. Since $b_n(s_i, s_j)$ is not available at this step, it is difficult to find the exact required $t(s_i, s_j)$. However, because $b_n(s_i, s_j)$ and $L(s_i, s_j)$ are highly correlated with each other, $b_n(s_i, s_j)$ can be estimated by modeling it with the average number of buffers corresponding to $L(s_i, s_j)$. Once $b_n(s_i, s_j)$ is estimated, $t(s_i, s_j)$ can be computed as described in Section V. The initial buffer type ($t_0$) for a given initial tree is computed as

$$t_0 = \text{Avg}_{s_i, s_j \in \Psi_0} t(s_i, s_j)$$

Once $t_0$ is determined, we adopt the fast variant of van Ginneken’s algorithm from [21] for initial buffer insertion. $b_n(s_i, s_j) \forall s_i, s_j \in \Psi$ is determined after initial buffer insertion and more accurate $t(s_i, s_j)$ can be obtained. For sink pairs that do not satisfy $\text{varEst}(s_i, s_j) < \Omega_{\Delta}$, we use the robustness-improvement algorithm from Section V to ensure that the tree eventually satisfies $\omega_{\Psi} < \Omega_{\Delta}$.

**V. ROBUSTNESS IMPROVEMENTS**

The initial buffer insertion algorithm cannot accurately estimate buffer types required for local-skew constraints for a given initial tree. Therefore robustness-improvement must follow after initial buffer insertion so that $\omega_{\Psi, \nu, \mu, \gamma} < \Omega_{\Delta}$ holds after all the skew optimization techniques are applied.

In an ideal situation in which we can reduce all the skew down to 0, $\text{varEst}(s_i, s_j) < \Omega_{\Delta} \forall s_i, s_j \in \Psi$ is sufficient to satisfy $\omega_{\Psi, \nu, \mu, \gamma} < \Omega_{\Delta}$. In practice we must estimate nominal local skew $\text{skew}_{\Psi}$ after accurate optimizations, which we upper-bound by 5ps based on experience.

**Theorem 2:** If $\text{skew}_{\Psi}$ is an upper bound of $\omega_{\Psi}$ and $\text{skew}_{\Psi} + \text{varEst}(s_i, s_j) < \Omega_{\Delta}$ for all $s_i$ and $s_j$ then $\omega_{\Psi, \nu, \mu, \gamma} < \Omega_{\Delta}$

$$\omega_{\Psi, \nu, \mu, \gamma} < \Omega_{\Delta}$$

The target buffer type for the tree-path between sink $s_i$ and $s_j$, $t(s_i, s_j)$ can be computed as the smallest $t$ such that

$$\Xi_{T, B, \nu} \cdot L(s_i, s_j), b_n(s_i, s_j), t] < \Omega_{\Delta} - \text{skew}_{\Psi}$$

From the above method, the minimum size of buffer type which satisfies $\text{varEst}(s_i, s_j) < \Omega_{\Delta} - \text{skew}_{\Psi}$ is selected to reduce capacitance. Once $t(s_i, s_j)$ is determined, the buffers in the tree path between sink $s_i$ and $s_j$ are substituted with type $t(s_i, s_j)$ buffers. This step is repeated for all eligible pairs of sinks within distance $\Delta$.

**VI. SKEW OPTIMIZATIONS**

In this section, several local skew optimization techniques are described. Each technique is designed to reduce skew under different circumstances, but the primary objective is to optimize the skew of given tree to below the local skew limit in the presence of variations. The target tuning amount for each edge of the tree can be determined by local-skew slack including variation modeling described in Section III.

### A. Wire snaking

Wire sizing and wire snaking are popular techniques for skew optimization and are often able to reduce global or local skew down to the practical skew limit. In this context, however, we exclude wire sizing because narrowing down a wire in the middle of a clock tree is risky due to the impact of variations. We extend the wire snaking technique from [14] to improve its speed and accuracy, while limiting its use of routing resources.

The optimal tuning amount for each edge can be obtained by the top-down slack computation explained in Section III-B. Let $T_{\text{target}}(e)$ be the amount of time in ps by which the edge $e$ must be delayed to achieve legal $\omega_{\Delta}$ under local skew constraints. $L_{\text{sn}}(e)$ denotes the length of the wire determined by the wire snaking algorithm to delay the edge $e$ by $T_{\text{target}}(e)$. Let $T_{\text{actual}}(e)$ be the amount of time in ps which the edge $e$ is actually delayed by $L_{\text{sn}}(e)$ of a wire. Ideally, the wire snaking algorithm can estimate $L_{\text{sn}}(e)$ so that $T_{\text{target}}(e) = T_{\text{actual}}(e)$. $L_{\text{ideal}}(e)$ is the length which satisfies $T_{\text{target}}(e) = T_{\text{actual}}(e)$. The total additional capacitance from wire snaking $\text{TotalCap}_{\text{sn}}$ is

$$\text{TotalCap}_{\text{sn}} = \sum_{e \in E} \kappa(L_{\text{sn}}(e_i))$$

where $\kappa(w)$ denotes the capacitance of a wire $w$, and the ideal total additional capacitance $\text{TotalCap}_{\text{ideal}}$ is

$$\text{TotalCap}_{\text{ideal}} = \sum_{e \in E} \kappa(L_{\text{ideal}}(e_i))$$

Practically, $T_{\text{actual}}(e) \neq T_{\text{target}}(e)$ unless extensive SPICE simulations are performed for finding $L_{\text{sn}}(e)$, which is unrealistic in terms of runtime for a clock network synthesis flow. When $T_{\text{actual}}(e) < T_{\text{target}}(e)$, another round of wire snaking is required to bring $T_{\text{actual}}(e)$ closer to $T_{\text{target}}(e)$. $L_{\text{sn}}(e)$ denotes the length of the wire determined at $i$th iteration of the wire snaking algorithm to delay the edge $e$. $T_{\text{actual}}(e)$ is the amount of time in ps by which the edge $e$ is actually delayed by $L_{\text{sn}}(e)$ of a wire. $T_{\text{target}}(e)$ is $T_{\text{target}}(e)$ when $i = 1$ and otherwise, it is $T_{\text{target}}(e) - T_{\text{actual}}(e)$. After $N$ iterations of wire snaking,

$$T_{\text{actual}}(e) = \sum_{i=1}^{N} T_{\text{actual}}(e)$$

where $\kappa(w)$ denotes the capacitance of a wire $w$, and the ideal total additional capacitance $\text{TotalCap}_{\text{ideal}}$ is

$$\text{TotalCap}_{\text{ideal}} = \sum_{e \in E} \kappa(L_{\text{ideal}}(e_i))$$

**Theorem 3:** $T_{\text{actual}}(e) \leq T_{\text{target}}(e)$ if and only if $\text{TotalCap}_{\text{sn}} \leq T_{\text{target}}(e)$ for every edge $e$ in the clock tree, then

$$\text{TotalCap}_{\text{sn}} \leq \text{TotalCap}_{\text{ideal}}$$

If the wire snaking algorithm over-estimates $L_{\text{sn}}(e)$ and results in $T_{\text{actual}}(e) > T_{\text{target}}(e)$ for any edge $e$ in any $i$th iteration, then $\text{TotalCap}_{\text{sn}}$ exceeds $\text{TotalCap}_{\text{ideal}}$ after all the iterations of the wire snaking algorithm because it means there exists excessive delay of a wire which results in an unrealistic in terms of runtime for a clock network synthesis flow.
in excessive delay of some sinks and possibly increases local skew around the sinks. Therefore the wire snaking algorithm must produce \( L_{sn}(e) \) which satisfies \( T_{i_{\text{actual}}}(e) \leq T_{i_{\text{target}}}(e) \) for optimized power consumption by the clock tree. However, if the gap between \( T_{i_{\text{actual}}}(e) \) and \( T_{i_{\text{target}}}(e) \) is too big, more iterations will be needed for \( T_{i_{\text{actual}}}(e) \) to approach \( T_{i_{\text{target}}}(e) \).

We improve the accuracy of wire snaking in two ways.

**Delay model for wire snaking.** To keep \( T_{i_{\text{actual}}}(e) \) \leq T_{i_{\text{target}}}(e) \) with optimal quality, we define \( \alpha \) where,

\[
\alpha \leq \frac{T_{i_{\text{actual}}}(e)}{T_{i_{\text{target}}}(e)} \leq 1.0
\]

Wire snaking algorithm aims for \( T_{i_{\text{actual}}}(e) \) to satisfy the above inequality with the highest \( \alpha \) possible. When \( \alpha \) is specified, the required worst-case number of iterations of wire snaking \( N \) to make \( T_{i_{\text{actual}}}(e) \) to \( T_{i_{\text{target}}}(e) \) within error rate \( \varepsilon \) is

\[
N = \left\lceil \log \left( \frac{\varepsilon}{\log(1-\alpha)} \right) \log e \right\rceil. \tag{13}
\]

Closed-form delay models like Elmore delay are not accurate enough to keep \( T_{i_{\text{actual}}}(e) \leq T_{i_{\text{target}}}(e) \) and \( \alpha \) high. To enhance the quality of estimation by the wire snaking algorithm, look-up tables for \( L_{sn}(e) \) are built by performing a set of SPICE simulations for each technology environment which includes technology model, types of buffers and wires, variation specification. In the simulations, \( T_{i_{\text{actual}}}(e) \) is tested with different snaking lengths on various locations of nodes in various types of clock trees. The results of simulations are stored in a look-up table, used by wire snaking during local skew optimization. We achieved \( \alpha \) values between 60% and 70%, therefore \( 4 \leq N \leq 6 \). Only one technology environment was used at the ISPD 2010 CNS contest, requiring a single set of simulations.

**Optimal node selection for wire snaking.** Figure 3 compares two different styles of wire snaking. Figure 3(b) illustrates undesired delay of sinks after wire snaking on non-buffer-output nodes. The increased capacitance and resistance by wire snaking affects the driving buffer which results in additional delay of slow sinks. Wire snaking at buffer output nodes, as in Figure 3(c), is much more accurate than wire snaking at any branch. Limiting wire snaking to buffer output nodes reduces the number of SPICE calls required for clock-tree tuning. This also reduces the number of simulations for building the look-up table by limiting the number of target nodes to be tested. Wire snaking usually increases slew rate of input nodes of downstream buffers. To prevent slew violation, slew rate numbers of downstream buffers are checked and if the worst slew rate is more than 70% of the given slew limit, the target node is excluded from wire snaking.

**B. Delay buffer insertion**

The local skew of a sink cluster driven by the same final buffer is often negligible. However, highly unbalanced sink capacitances or layout obstacles in those clusters can result in significant local skew. An alternative technique is needed because wire snaking in Section VI-A is inapplicable. In this case, inserting a buffer at the target node is very efficient for two reasons. First, skew can be reduced by the delay of the inserted buffer. Second, further precise wire snaking is possible because the inserted buffer isolates the target node from the remainder of the cluster.

Let \( W(B) \) be the set of sinks driven by a final buffer \( B \) and \( d(B) \) be the delay of the buffer \( B \). Delay buffer insertion is required if there exists \( s_i, s_j \in W(b) \) where \( \text{skew}(s_i, s_j) + \text{varEst}(s_i, s_j) \cdot \Omega_\Delta > d(B) \).

For each path from the buffer to the sinks, inserting at most one buffer is sufficient since the wire snaking algorithm in Section VI-A can be invoked again at the output node of inserted buffers. Figure 4 illustrates delay buffer insertion algorithm followed by wire snaking. When a delay buffer is inserted, it is placed at the node so that the input capacitance of a delay buffer is comparable to the sum of downstream sink and wire capacitance of the target node, thus sink latency in the other path changes very little. (see Figure 4 (b)).

![Fig. 3. Comparison of different wire snaking strategies to satisfy \( \Omega_\Delta = 10\mu s \). (a) Unoptimized sink latencies are shown. 20\mu s of additional delay is required for the left sink. (b) Wire snaking at non-buffer output nodes results in undesired delay at the right sink. (c) The snaked wire is isolated from the right sink by the left buffer, therefore only the left sink is delayed and \( \omega_\Delta \) satisfies local skew constraints.](image)

![Fig. 4. Delay buffer insertion and subsequent wire snaking when \( \Omega_\Delta=10\mu s \), the delay of the buffer \( d(B)=10\mu s \). (a) Unoptimized sink latencies are shown. (b) Delay buffer insertion for skew reduction and isolation of the target node. (c) The snaked wire is isolated from the right sink by the delay buffer.](image)

![Fig. 5. Our clock tree for *isp10cns07*. Sinks are indicated by crosses, buffers are indicated by blue rectangles. \( \Delta = 600\mu m \) is indicated at the left-bottom of the figure.](image)
VII. Empirical validation

Our implementation, Contango 2.0, is written in C++ and is based on our software Contango 1.0 [14] that shared the first place at the ISPD 2009 clock-network synthesis contest. Contango 2.0 was the sole winner of the ISPD 2010 contest, but we now report significantly stronger results.

**ISPD 2010 benchmarks.** Table II lists the statistics of all benchmarks from the ISPD 2010 contest. The contest limited slew to 100 ps., and all reported clock networks satisfy this constraint. Slew in Contango 2.0 trees do not exceed 81 ps. Table III compares Contango 2.0 with CNSrouter and NTUclock. Clock networks produced by our software have smaller capacitance than CNSrouter and NTUclock on average by 4.22× and 4.13× respectively. The contest imposed local skew constraints with yield y = 95%. Our clock trees always yield > 95%, while CNSrouter violates yield constraints on three benchmarks and NTUclock on all benchmarks except one. All three teams satisfied the 12-hour runtime limit for all benchmarks. Our data suggest that wire snaking usually increases wire length by 1-3% (5.43% in one case), which is small enough to neglect the negative effects of wire snaking. Figure 7 compares probability density functions (pdf) produced by Monte-Carlo SPICE simulations of our clock trees to those of clock meshes produced by CNSrouter. One such clock tree is illustrated in Figure 5. Despite the dramatic differences in network topology and total capacitance between trees and meshes, some of the plots in Figure 7 bear striking resemblance (cns01, cns02, cns04, cns05). To explain this phenomenon, we recall that meshes cannot be buffered directly resemblance (cns01, cns02, cns04, cns05). To explain this phenomenon, we recall that meshes cannot be buffered directly and are therefore driven by a buffered clock tree. Such a clock tree can be constructed by the same DME algorithm that we use, which is why the pdf profiles in Figure 7 reflect the pointset of sink locations. Apparently, the mesh does not significantly change this profile.

**Power versus robustness to variations.** Figure 6 describes experiments on benchmark ispd10cns08 with different local skew constraints. When tight local skew constraints are given, large buffers are required to ensure robustness to variations, increasing the capacitance of the clock tree. On the other hand, a large portion of capacitance can be saved when local skew constraints are loose. To clarify the impact of variation, we plot variational skew (y-axis), defined as $\omega_{\Delta, \nu, y} = \omega_{\Delta}$ for $\Delta, \nu, y$ from Table II.

VIII. Conclusions

Power-performance-cost trade-offs are becoming a major issue in modern high-performance CPU clock designs. Mesh structures often sacrifice power to improve robustness to variations. We propose a tree solution for CPU clock routing that improves power consumption under tight skew constraints in the presence of variations. To this end, we introduce the notion of local-skew slack for clock trees, a model for variational skew, a path-based technique to enhance robustness, a new time-budgeting algorithm for clock-tree tuning and accurate optimizations that satisfy budgets. We have shown that clock trees can be tuned to have nominal skew below 5 ps and total skew in single picoseconds in the presence of variations. Our optimizations not only satisfy given skew constraints and target yield but also lead to 4.22× capacitance improvement on average over mesh structures proposed in the ISPD 2010 contest. Furthermore, our clock trees had a higher yield than the meshes because meshes are not as easy to tune for nominal skew. Our analysis does not consider gated clocks, inductive effects and short-circuit power in meshes, but these factors generally favor trees over meshes. Our strong empirical results suggest that clock trees constructed using accurate variational skew modeling and optimizations have distinct advantage in power consumption and similar robustness as meshes. Hence, our techniques may improve power of future CPUs without sacrificing other performance metrics.

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REFERENCES


### ISPD’10 Results on the ISPD 2010 Contest Benchmark Suite

Skew numbers are reported in pF, capacitance in pF and CPU time in s. The numbers in parentheses of the capacitance column refer to the fraction of capacitance of the snaked wires in %. Skew constraint violations are shown in strikethrough font. Otherwise, skew results are not comparable because skew can be traded for capacitance, which was the primary objective of the contest. All networks produced by these tools satisfy slew constraints imposed at the ISPD 2010 contest. Due to limited page space, we do not include results for the other teams, but significantly outperform them in solution quality.

<table>
<thead>
<tr>
<th>Bench.</th>
<th>CNSrouter 3/16/2010</th>
<th>NTclock 3/16/2010</th>
<th>Contango 2.0 4/14/2010</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td>Mean</td>
<td>Skew+Var</td>
<td>Total</td>
</tr>
<tr>
<td>cns01</td>
<td>5.27</td>
<td>7.32</td>
<td>841.2</td>
</tr>
<tr>
<td>cns02</td>
<td>6.27</td>
<td>4.24</td>
<td>1454</td>
</tr>
<tr>
<td>cns03</td>
<td>2.07</td>
<td>2.70</td>
<td>162.5</td>
</tr>
<tr>
<td>cns04</td>
<td>2.83</td>
<td>3.98</td>
<td>277.1</td>
</tr>
<tr>
<td>cns05</td>
<td>2.88</td>
<td>4.38</td>
<td>175.5</td>
</tr>
<tr>
<td>cns06</td>
<td>12.38</td>
<td>144.6</td>
<td>133.3</td>
</tr>
<tr>
<td>cns07</td>
<td>12.39</td>
<td>12.24</td>
<td>390.2</td>
</tr>
<tr>
<td>cns08</td>
<td>6.15</td>
<td>7.33</td>
<td>222.8</td>
</tr>
</tbody>
</table>

Relative Mean 4.22 4.13 1.0

### Tables

#### Table III

<table>
<thead>
<tr>
<th>Bench.</th>
<th>CNSrouter 3/16/2010</th>
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<th>Contango 2.0 4/14/2010</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td>Mean</td>
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<td>Total</td>
</tr>
<tr>
<td>cns01</td>
<td>5.27</td>
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<td>841.2</td>
</tr>
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<td>6.27</td>
<td>4.24</td>
<td>1454</td>
</tr>
<tr>
<td>cns03</td>
<td>2.07</td>
<td>2.70</td>
<td>162.5</td>
</tr>
<tr>
<td>cns04</td>
<td>2.83</td>
<td>3.98</td>
<td>277.1</td>
</tr>
<tr>
<td>cns05</td>
<td>2.88</td>
<td>4.38</td>
<td>175.5</td>
</tr>
<tr>
<td>cns06</td>
<td>12.38</td>
<td>144.6</td>
<td>133.3</td>
</tr>
<tr>
<td>cns07</td>
<td>12.39</td>
<td>12.24</td>
<td>390.2</td>
</tr>
<tr>
<td>cns08</td>
<td>6.15</td>
<td>7.33</td>
<td>222.8</td>
</tr>
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Relative Mean 4.22 4.13 1.0

### Fig. 7

Probability density functions for worst local skew of our clock trees (blue line) and meshes produced by CNSrouter (gray dashed line) for the eight ISPD 2010 benchmarks, calculated using 500 independent SPICE runs for each benchmark. The x-axis shows skew in picoseconds. Local skew limits (Ω) are shown with red solid lines, and the 95%-ile of local skew (Ω, ν) are shown by dotted green lines (our work) and dashed gray vertical lines (CNSrouter).

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