Design of Analog Circuits Using Organic Field-Effect Transistors

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***Abstract*–Organic field-effect transistors (OFETs) can be manufactured at low temperatures, enabling the fabrication of integrated circuits on flexible plastic substrates and the coverage of large areas at potentially low cost. This paper evaluates state-of-the-art OFET technology from the perspective of the analog circuit designer. Specifically, we review important OFET device performance metrics in comparison to generic silicon CMOS transistors. In addition, an overview of recent accomplishments in OFET-based analog design is presented.**

I. Introduction

Over the past several decades, the functionality provided by integrated circuits in silicon technology has changed the way we live and communicate. Today's silicon CMOS technology delivers an immense computing power, measured in terms of logic gate density and energy per logic operation. In addition, this technology can be used to realize high-performance analog signal processing functions that interface with real world physical signals.

As the success of silicon-enabled devices lives on, a new class of applications is emerging, demanding electronic circuit films that can span large areas and provide mechanical flexibility or even stretchability [1]. Examples include active-matrix displays, electronic paper, active clothing, smart packaging of consumer products, health monitoring devices, and sensory skin for robotics. Today, organic semiconductor thin-film technology is viewed as a promising candidate for meeting the requirements of these applications. Because OFETs can be manufactured at or near room temperature, they allow integrated circuits to be made on flexible plastic substrates that do not withstand the high processing temperatures used for silicon based devices. Furthermore, the ability to print organic OFETs advances the prospect of inexpensive large-area electronics [2].

As illustrated in Fig. 1, most electronic systems can be partitioned into an analog front-end that contains signal condition functions (e.g., signal amplification, filtering, power amplification), data converters (analog-to-digital and digital-to-analog), as well as a digital computing backbone. In the context of the emerging applications discussed above, the analog front-end circuitry may interface with radio frequency identification (RFID) antennas [3], vapor sensors [4], PH sensors [5], temperature sensors [6], pressure sensors [7], light emitting diodes [8], polymer actuators [9], and so on.

This paper evaluates state-of-the art OFET technology from the perspective of the analog interface circuit designer (Section II) and provides an overview of recent accomplishments in analog OFET circuit design (Section III).

II. OFET Characterization

In recent years, various options for the material systems and process flow for OFETs fabrication have been explored. The process described in [10] was used to fabricate 10-V RFID circuits on flexible plastic substrates using p-channel OFETs with a minimum channel length of 5 μm and a carrier mobility of 0.5 cm^2/Vs. The process used in [11] provides 5-μm p-channels with a carrier mobility of 0.05 cm^2/Vs and threshold voltages on the order of -3 V. This technology has been used to demonstrate circuits operating at supply voltages near 20 V. As a basis for the discussion in this section, we will utilize the parameters of a low-voltage process using ultra-thin gate

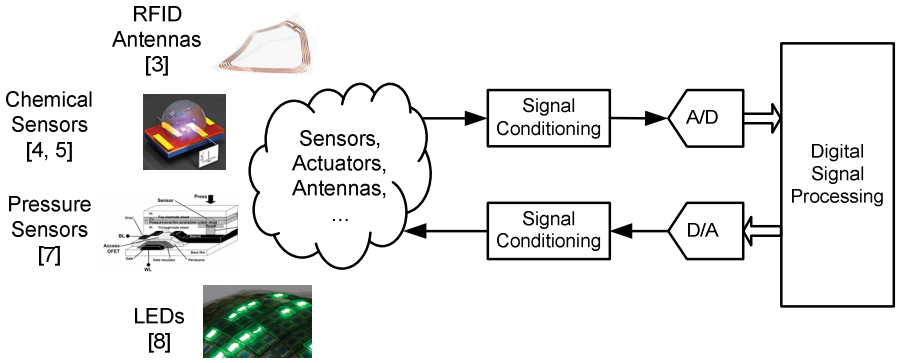

Fig. 1. General block diagram of a mixed-signal electronic system, including examples of front-end transducers used in emerging OFET applications.

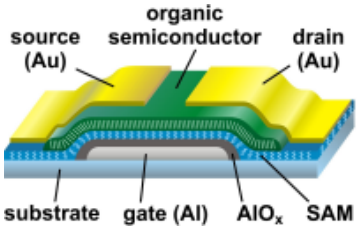

Fig. 2. Structure of the organic field effect transistors described in [12].

dielectrics that allows OFET circuits to operate at supply voltages of 2-3 V [12, 13, 14]. This technology provides both p- and n-channel transistors with minimum gate lengths of 20 µm. The cross-section of a transistor fabricated in this technology is shown in Fig. 2 and selected transistor parameters are summarized in Table 1. Most notable here is the large gap in mobility between the n- and p-channel transistors. Air-stable n-channel transistors are still under active development and have not yet reached the same level of performance as their p-type counterparts. Also, note that the channel overlap ($L_{overlap}$) is comparable to the channel length itself; this is due to the relatively imprecise shadow masking used in the definition of the device features.

TABLE I
Typical OFET Technology Parameters

Parameter	Symbol	Value
Supply Voltage	V_{DD}	3 V
Minimum channel length	L_{min}	20 µm
Channel overlap	$L_{overlap}$	20 µm
Gate dielectric capacitance	C_{ox}	7 fF/µm^2
p-channel molecule	DNTT	
n-channel molecule	F_{16}CuPc	
p-channel mobility	μ_p	0.6 cm^2/Vs
n-channel mobility	μ_n	0.02 cm^2/Vs
p-channel threshold voltage	V_{tp}	-0.5 V
n-channel threshold voltage	V_{tn}	0.5 V

Depending on how the transistors are used in a circuit, various secondary, design-centric performance metrics can be extracted from this data. For instance, in display applications, the transistors' on/off current ratio may be of primary importance. In the following sub-sections, we will evaluate metrics that pertain more specifically to the design of signal conditioning and data conversion circuitry.

A. Transconductor application

For transistors that are meant to operate as transconductors in linear circuits (such as operational amplifiers), three primary figures-of-merit can be used to assess a transistor's performance: (a) g_m/I_D, quantifying how efficiently the drain

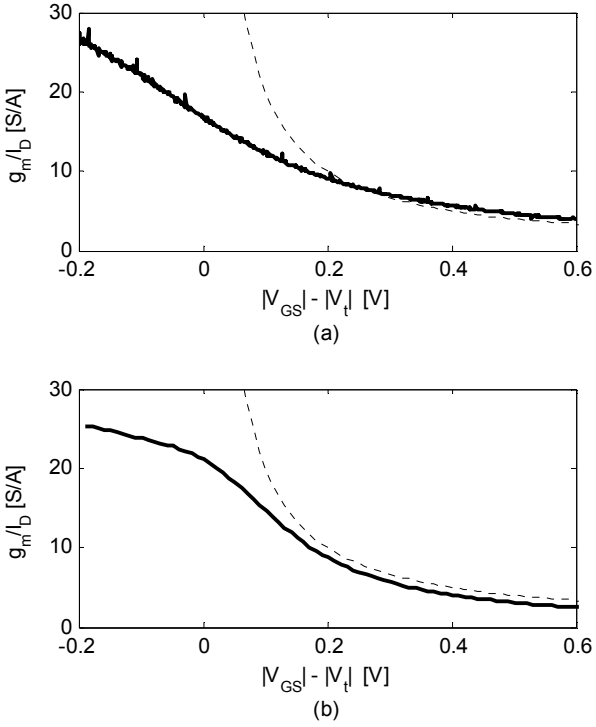

Fig. 3. Transconductor efficiency g_m/I_D for (a) a p-channel OFET (measured), in comparison with (b) a typical 0.35-µm n-channel silicon MOSFET (simulated). The dashed lines correspond to the square law expression $g_m/I_D = 2/(V_{GS}-V_t)$.

current is utilize to generate transconductance, (b) g_m/C_{gg}, quantifying how much transconductance is obtained in exchange for undesired gate capacitance, and (c) g_m/g_{ds}, representing the transistor's intrinsic small-signal voltage gain.

Measured data for the transconductance efficiency g_m/I_D of a p-channel OFET are shown in Fig. 3(a). The observed characteristic is similar to that of a typical 0.35-µm silicon MOSFET, shown in Fig. 3(b) for comparison. At large $V_{GS}-V_t$, g_m/I_D approaches $2/(V_{GS}-V_t)$, as predicted by the basic square law equations. The curves deviate from the square law characteristic for small $V_{GS}-V_t$, as the device operates in moderate inversion. In weak inversion, the upper bound on g_m/I_D is given by q/nk_BT, where n is the so-called nonideality factor, which also defines the subthreshold slope of the transistor.

The parameter $f_T = g_m/2\pi C_{gg}$, also known as the transistor's cutoff frequency, is plotted in Fig. 4. As expected, due to its low mobility and long channel length, the OFET achieves an f_T that is roughly 6 orders of magnitude below that of a 0.35-µm silicon MOSFET. Once a transistor's f_T is known, it is possible to estimate approximate bounds on the maximum frequency that various circuits can achieve. Continuous time amplifiers tend to be feasible up to signal frequencies of $f_T/10$. Feedback amplifiers in switched capacitor circuits are known to operate at sampling frequencies up to $f_T/50$. Assuming $f_T \cong 10$ kHz, the corresponding frequency range for a classical transconductor-based circuit is approximately 200 Hz – 1 kHz. These numbers

are sufficient for the low-frequency sensor signals seen in many of the applications discussed in Section I.

When larger operating frequencies are desired, it becomes necessary to increase the mobility and/or use shorter channel lengths. This is evident from the following expression that holds for square-law transistors

$$f_T = \frac{1}{2\pi}\frac{g_m}{C_{gg}} = \frac{1}{2\pi}\frac{3}{2}\frac{\mu(V_{GS}-V_t)}{L^2}\frac{1}{\left(1+3\frac{L_{overlap}}{L}\right)} \qquad (1)$$

The rightmost term in this equation (containing $L_{overlap}$) has been negligible for all but the most recent nanometer CMOS technologies. In out OFET process, the term is significant due to $L_{overlap} \cong L$, causing a 4x degradation in f_T.

In contrast to transit frequency, the intrinsic gain of state-of-the-art OFETs is currently not being perceived as a limit factor. Due to the relative long channels, the intrinsic gain of the transistors discussed here are on the order of 200 – 400. This is substantially larger than the intrinsic gain of short channel silicon MOSFETs, which are on the order of 5 – 50.

B. Analog switch application

In analog circuits based on charge redistribution, FETs are employed as sampling and redistribution switches. In this application, the on-resistance of the transistor in the triode region becomes important. Fig. 5 shows measured data for the on-resistance of a 200 µm/20 µm p-channel OFET versus V_{GS}. Assuming that the circuit operates near mid-supply, an average on-resistance on the order of 100 kΩ is to be expected. With C_{gg} = 84 pF, the self loaded time constant of this switch is then $RC_{gg}/2$ = 4.2 µs. Assuming that the circuit must settle for 10 time constants within ½ clock cycle, the maximum clock frequency follows as approximately 11 kHz. As expected, this number is significantly higher than the bound obtained for transconductor based circuits.

Unfortunately, owing to the thin gate oxide used in the assumed technology, there also exists a lower bound for the switching frequency in charge-processing circuits. As discussed in [13], the minimum update frequency for charge storage nodes loaded with thin gate-oxide is on the order of 10 Hz (depending on the desired precision). This is somewhat troublesome for OFET circuits, since the upper frequency of operation is also relatively low, leaving only a few decades of frequency to work with.

C. Power switch application

As evident from the numbers in Fig. 5, it is difficult to achieve small on-resistances in current OFET technology. For the transistor characterized in the previous sub-section, assuming V_{GS} = 3 V and V_{DS} = 2 V, a current of approximately 40 µA is obtained. A 6x wider transistor was used in [15] to drive a low-power LED. Even though OFET mobilities are expected to improve in the future, an interesting alternative for high current drivers may lie in electrochemical switches [16]. These devices provide substantially higher currents, albeit at lower switching speeds (on the order of seconds).

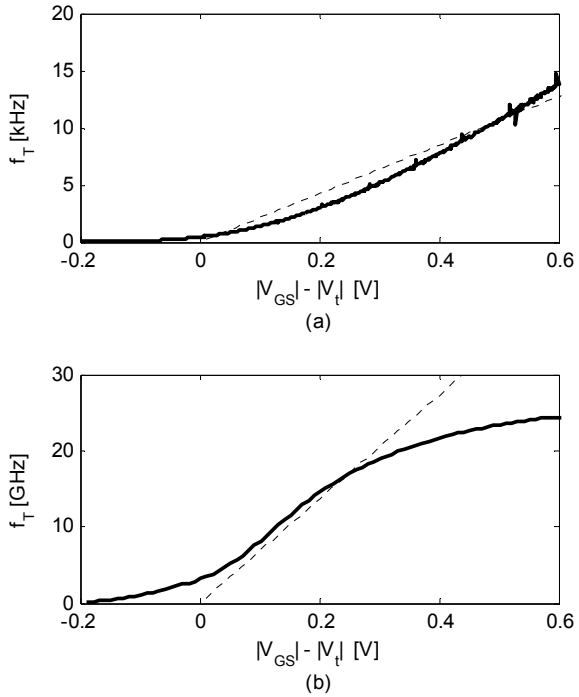

Fig. 4. Transit frequency for (a) a p-channel OFET, in comparison with (b) a 0.35-µm n-channel Si MOSFET (simulated). The dashed lines correspond to a square law fit. The OFET plot was constructed using measured transconductance data and estimated capacitance values.

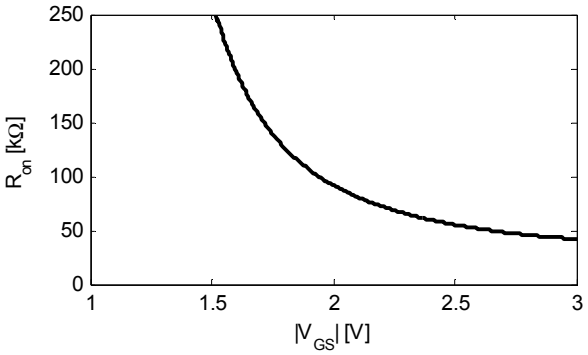

Fig. 5. Measured R_{on} of a 200 µm/20 µm p-channel OFET. (V_{DS}=-0.1 V).

D. Variability considerations

In the thin-film processes assumed in this discussion, the use of shadow masks and non-uniformities in device mobility introduce significant mismatches between nominally identical transistors made in the same fabrication run. As shown in Fig. 6, measurement of 60 p-channels and 60 n-channel OFETs on the same substrate show 1-σ saturation current mismatches of 39% and 23%, respectively. At present, this prohibits the use of these OFETs in configurations that rely on precisely matched currents, as for instance current-steering D/A converters.

III. Analog Circuit Developments

In this section, we will provide a (non-exhaustive) overview on recent developments in the design of analog circuits using OFET technology. The first linear amplifier circuits using OFETs were described in [17, 18], trailing numerous publications dealing mostly with RFID tags and support circuitry for displays. The first organic voltage comparator, operating at 1 kHz was published in [19], laying the foundation for more complex interface circuit components such as data converters.

Subsequently, our research group demonstrated a 6-bit organic D/A converter [13] based on charge redistribution. This design exploits the fact that the capacitors available in our thin-film technology exhibit better matching than OFETs. Combining this D/A converter with a multi-stage, auto-zeroed voltage comparator resulted in the 6-bit A/D converter design described in [14]. This converter is clocked at 100 Hz, and achieves a conversion rate of 16.7 samples/sec, dissipating 3.6 µW from a 3-V supply.

At the same time, the authors of [20] showed that active charge integrators can be realized in their technology. These integrators were used to form the first delta-sigma modulator in OFET technology achieving a signal-to-noise ratio of 26.5 dB for a signal bandwidth of 17 Hz. This design dissipates 1.5 mW from a 15-V supply.

IV. Conclusion

Analog circuit design using OFETs is at an inflection point where several of the basic circuit architectures have been demonstrated in experiment. Today's OFET technology is capable of processing signals up to frequencies in the kilohertz range, which already meets the requirements of several sensor-centric applications. The future will bring improvements in fabrication technology, enabling larger device counts and higher mobility. In addition, the potential heterogeneous integration with technologies of complementary strength is seen on the horizon as an interesting opportunity [21].

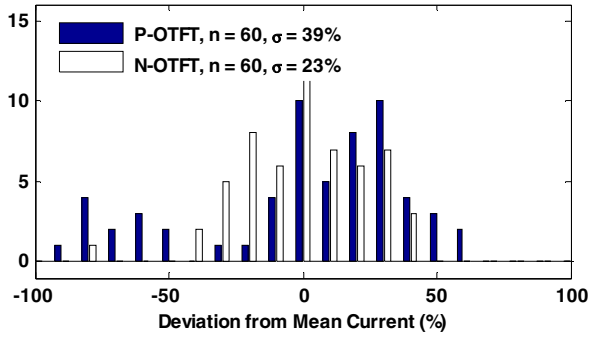

Fig. 6. Measured distribution of OFET saturation current mismatches.

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