Structured Analog Circuit Design and MOS Transistor Decomposition for High Accuracy Applications

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Abstract—This paper addresses the problem of transistor decomposition, which can be used in high accuracy analog applications and structured analog design. We made a test chip to verify the feasibility of the transistor decomposition because of the lack of theoretical support. The DC/AC measurement results from the chip suggests that the decomposition, the transistor channel tuning, as well as structured analog design based on the transistor array are applicable. Also our test chip shows that design with transistor array can suppress the variation of $V_{th}$ stemmed from CMP process. Based on this conclusion, we propose a simple framework with transistor array for structured analog layout generation, which involves the transistor decomposition. Using this framework, we generate several layouts for a typical CMOS OPAMP circuit and compare the automatically generated layouts with the manual layouts. Although the layout sizes of the transistor array based OPAMPs are slightly bigger than that of the manual designs, the automatic layout generation is much faster than manually synthesizing the layout.

I. INTRODUCTION

As IC design advances to nano-scale era, the process-induced variation is becoming an unneglectable problem. According to [1], up to 30% of transistor variation has been observed in the 90 nanometer process ICs. Many works have been reported in the past several years to tackle this problem [2] [3] [4] [5]. Most of them devoted to the digital IC design since the process-induced variation degrades the performance so significantly that the benefit of small feature size may be totally overwhelmed, for example, makes the chip run at a low speed.

The analog ICs, whose performance may not benefit from the small feature size as much as of digital ICs though, also suffer from the process-induced variation. In order to handle this problem, the analog circuit designer usually attaches some external circuits to the analog ICs, which, to some degree, can recover the performance degradation. Recent development of analog IC design involves the post-silicon tuning to deal with the process variation, especially for the high accuracy applications. Since the process variation causes the channel length and width of a transistor to differ from their design values, the post-silicon tuning is resorted to fix these errors. Obviously, physically adjusting the channel length and width is not an easy job since without the chip fabricated as yet, we even don’t know how bad the variation is. While with the chip fabricated, we can hardly touch the transistor that should be adjusted. The ways in which to circumvent this paradox basically fall into two categories: one is putting some spare circuits in the chip along with the circuits concerned, and connecting these circuits with the external connections if necessary [6] [7]. The other way is providing adjustable bulk voltages or power supply for the selected transistors [6] [8] [9] [10], for example, giving the independent bulk voltage supply to different circuits.

In this paper one of the topics that will be covered is the transistor decomposition. It can be employed for direct fine grained adjustment of the channel length/width of the selected transistors. This fine grained adjustment can be used in the post-silicon tuning for the high accuracy analog applications.

Another topic that will be addressed is the structured analog ICs design using an array of fine grained transistors. It is well known that the design automation for analog ICs, except for several programs such as SPICE-like simulation tools, is still far away from maturity compared to the design automation tools for digital circuits. Many works focusing on digital design, ranging from front-end logic synthesis to back-end physical design, have been published in past 40 years and been successfully applied to the digital IC design tools. However due to its sensitivity to noise and thermal distribution, the analog circuit can hardly borrow these algorithms without extensive modification. The major barrier to absorb these algorithms is that the behavioral model of analog circuits quite differs from digital circuits, and strongly depends on the geometric dimensions of the circuits’ elements.

In hope of utilizing those sophisticated algorithms of digital circuit design, we use an array of the transistors with unified channel length and unified channel width to simulate the gate array of digital design, and manage to replace all the transistors in the analog circuits with these unified transistors. With such a well-structured design, it is possible to employ the algorithms of the digital design, for example, the channel routing algorithm [11], to aid the designers.

A key problem is the feasibility of replacing all the transistors in the circuit with the unified transistors, especially for those transistors with the channel length different from that of unified transistor. To verify the feasibility, we made a test chip with the unified transistor array in it, and measured the DC/AC behaviors of the transistor array based circuits.

In addition to easing the modification to the algorithms of the digital circuit design, one of the merits brought by this structured layout is its excellent ability to implement the symmetrical/common-centroid placement, which is believed to

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be very important in the analog design [12] [13]. What’s more, with this well-organized structure, the CMP (Chemical Mechanical Polishing)-induced process variation can be alleviated [14] [15] [16].

Our contribution in this paper can be summarized as follows:

- We propose a transistor decomposition method for structured analog IC design. It can be used in the post-silicon tuning to compensate for the process variation-induced performance degradation for high accuracy analog applications.
- A test chip is made to verify the feasibility of the transistor decomposition by measuring the DC/AC behaviors of the circuits in the chip.
- A framework of structured analog IC layout design is proposed by using the transistor decomposition and transistor array. According to the measured results from the test chip, design with transistor array can effectively suppress the variation caused by CMP.

The rest of this paper is organized as follows. Section II gives the preliminaries regarding the transistor decomposition and the transistor array. Section III analyzes the DC/AC behaviors of the circuits using the transistor decomposition. Section IV discusses design with transistor array and proposes a framework of analog layout generation with the transistor array. Section V compares the area of manual design and automatic design. Section VI concludes the paper.

II. PRELIMINARIES

The process induced variation will cause the channel length $l$ and channel width $w$ of a transistor to differ from its design values. In the analog IC, this variation may lead to a matching problem. For example, a current mirror usually needs the same $l$, but $M_1'$ has a smaller $w$ and is for tuning the channel width of $M_1$. Transistor $m_1$ and $M_1$ have the same $w$, but $m_1$ has a smaller $l$ and is for tuning the channel length of $M_1$. When using $D_1$ as the drain, $G$ as the gate, and $S$ as the source of a transistor, the circuit functions as a normal MOS transistor. If we connect $D_1$ and $D_3$ together as the drain, the circuit functions as a transistor with $w = w_{M1} + w_{M1'}$. If using $D_2$ as the drain, the circuit functions as a transistor with $l = l_{M1} + l_{M1'}$ provided the transistor decomposition in the channel length direction is applicable.

Since $I_{ds}$ is a linear function of $W$ and a nonlinear function of $L$ in Eq.(1). However if we reconsider the $L$-decomposition and re-connection from a point of physical view, the entire procedure should not have caused such a big difference as Eq.(1) implied provided ignoring the tiny resistors and capacitors introduced by the serial re-connection, and assuming that the decomposition line is perpendicular to the channel edge in the channel length direction (See figure 2).

![Fig. 1. Channel length and width tuning. Transistor $M_1$ and $M_1'$ have the same $l$, but $M_1'$ has a smaller $w$ and is for tuning the channel width of $M_1$. Transistor $m_1$ and $M_1$ have the same $w$, but $m_1$ has a smaller $l$ and is for tuning the channel length of $M_1$. When using $D_1$ as the drain, $G$ as the gate, and $S$ as the source of a transistor, the circuit functions as a normal MOS transistor. If we connect $D_1$ and $D_3$ together as the drain, the circuit functions as a transistor with $w = w_{M1} + w_{M1'}$. If using $D_2$ as the drain, the circuit functions as a transistor with $l = l_{M1} + l_{M1'}$ provided the transistor decomposition in the channel length direction is applicable.](image1)

![Fig. 2. Physical view of transistor decomposition. (a) Transistor without decomposition. (b) Transistor decomposition without connection-introduced resistance and capacitance. (c) Transistor decomposition with connection-introduced resistance and capacitance.](image2)

The transistor assembled by these sub-transistors in the serial manner should only be slightly different from the original. Unfortunately, as far as we know, there is no such research on the decomposition of channel length being reported. In order to verify our guessing, we made a test chip and had some transistors $L$-decomposed in the chip. The assembled transistors are then conducted to the DC/AC analysis.

If the idea of transistor decomposition works, we can also use an array of decomposed transistors to generate structured layout for analog circuit design.

Since one of our research motivations is to ease applying those sophisticated algorithms of digital circuit design to analog circuit design, we want to standardize the elementary components in the analog circuits as we are doing in digital circuit design, such as using the standard cells or gate-array as the basic design elements. However, it is well known that there is no such an elementary component in the analog circuits, except for MOS transistor, playing the similar role as a standard...
cell in digital circuits. Even for the transistors, their channel length and/or channel width vary largely, not only in chip level but also in sub-circuit level. But this phenomenon rarely happens in the digital circuit design. If we can decompose the transistor into a set of standard transistors with unified channel length \( L_u \) and unified channel width \( W_u \), called unit-transistors, in the circuit level, the circuit can be built on these elementary components, called Transistor Array (TA for short, see Figure 3 for example.) One of the important reasons we employ the transistor array is that, according to the measured results from our test chip, we found that the transistors with different layout structures show more significant spatial-dependent variation in the threshold voltages \( V_{th} \) than the transistors with the same structure (Refer to figure 5). Therefore we can use the transistors with unified channel length and channel width to alleviate the spatial-dependent variation of \( V_{th} \).

Another reason is that, if, ideally, all the transistors in the circuit are successfully replaced with the unit-transistors, we can easily obtain a well-structured placement since all the unit-transistors can be arranged on an uniform grid (See Figure 4). With such a gate-array-like placement, we have a great opportunity to make use of the routing techniques of digital circuit to route analog circuits, since the routing channels can be easily defined. Another good feature of this structured placement is that it can easily import the layout constraints, such as symmetrical constraints or common-centroid constraints, during the placement generation.

Also with a transistor array based structure, We can obtain a better post-0.3MP profile (see figure 6), which can even the STI-stress up [17] to reduce the process-induced variation.

III. TRANSISTOR DECOMPOSITION

In order to verify the idea of transistor decomposition, we made a test chip and put some \( L \)-decomposed transistors in it, to perform the DC analysis and AC analysis. Please note that we are not going to perform the DC/AC analysis on the \( W \)-decomposed since it widely proved applicable.

A. DC Analysis of Transistor Decomposition

The circuit for DC analysis is as shown in figure 7. All the transistors’ gates are connected to the same voltage, and each gate is controlled by a transfergate. Each time only one transfergate is switched on to provide the gate voltage \( V_{gs} \). In the circuit, there are 3 transistors in essence, and all the 3 transistors share the same \( V_{ds} \). The left most transistor is the one without transistor decomposition. The one in the middle is decomposed into two unit-transistors, and each of the unit-transistors has a half of the channel length of the left most transistor. The right most transistor is decomposed into 4 unit-transistors, and each of them has a quarter of the channel length of the left most transistor.

By varying \( V_{gs} \) and \( V_{ds} \), we can measure the drain-source current \( I_{ds} \) as shown in Figure 8. According to the measured \( I_{ds}, V_{th} \) curves from the chip, we can see that in spite of the small difference between these curves, in the DC analysis, the idea of \( L \)-decomposition works very well. The
small difference in $I_{ds}$ may be caused by the decomposition-introduced resistance, i.e., the small resistance introduced by the serial connection. Since the more unit-transistors the original transistor is $L$-decomposed into, the more resistance the decomposition introduces, and the smaller the $I_{ds}$ is under the same $V_{gs}$ and $V_{ds}$. The measurement results also suggest that the channel length modulation effect, which may have impact on a single unit-transistor though, does not show too much difference between the original transistor and the one assembled by the unit-transistors.

B. AC Analysis of Transistor Decomposition

In order to analyze the AC behavior of the decomposition, we build a simple common source amplifier using the transistors (see figure 9). The resistors $R_1$ and $R_2$ are used to bias the transistors to work in the strong inversion region. $V_{in}$ is an input sine wave to be amplified. By inputting a sine wave of 50KHz into the amplifier, we can observe that the signal is successfully amplified by all the 3 amplifiers when switching one transistor’s gate on each time (see figure 10(a), (b) and (c)).

Please note that we are not discussing how to design a good common-source amplifier here, but trying to tell how much difference the decomposition will cause for an amplifier under the same biasing voltage and load.

Figure 11 shows the gain bandwidth plots of the 3 amplifiers. We can see that the amplifiers with decomposed transistors have lower gains. This is because the transistor assembled by the unit-transistors has bigger on-resistance $r_o$ due to the contribution of the connection, and the gain $A$ depends on the transconductance $g_m$:

$$A = -R_d g_m$$

where $g_m$ depends on the value of $I_{ds}$ under the gate biasing voltage, i.e., the source-drain current of DC operation point:

$$g_m = \sqrt{\frac{2W}{L}KL_{ds}}$$

$K$ is a process-related parameter, and remains constant for the 3 amplifiers. As suggested by equations (2) and (3), smaller $I_{ds}$ causes smaller gain. As we observed in the DC analysis, $I_{ds}$ will decrease when decomposing the original transistor into more unit-transistors, thereby leading to a smaller gain.

Also we can observe that as the number of the unit-transistors increases, the bandwidth decreases as well. This
may be caused by the decomposition-introduced parasitic capacitance.

Good news is that, in spite of the AC/DC behavioral difference existing due to the transistor decomposition, it is so small that the $L$-decomposition is applicable in the channel length tuning and design with the transistor array.

**IV. FRAMEWORK OF STRUCTURED ANALOG DESIGN WITH TRANSISTOR ARRAY**

Since our test chip has proven the feasibility of design with the transistor array in the analog circuit design, now we propose a simple layout generation framework for the analog circuit with the transistor array.

It’s notably that in this paper we actually use a row-based style to generate the layout (see figure 12), i.e., all unit-transistors are grouped into rows and laid row by row. The unit-transistors in the same row must share the same bulk potential. The layout in this style is thought of as a placement with regular bulk structure. The reason that we use this layout style lies in the two observed facts:

- There are few different bulk potentials other than $V_{OD}$ and $V_{GND}$.
- The transistors supposed to be matched are very likely to having the same bulk potential.

Therefore the unit-transistors belonging to the matched transistors will be arranged into same rows, and we can solve the matching problem row by row by elaborately arranging the corresponding unit-transistors, which leads to one more good feature: in each row, we only need to deal with a simplified one-dimensional constraint-driven placement, for example 1-D symmetrical/common-centroid placement problem.

- **A. Choosing $l_u$ and $w_u$ for Unit-transistor**

To use the transistor array to generate the layout, we have to choose the proper values of channel length and channel width for unit-transistor, and for each transistor in the circuit, we will use a certain number of unit-transistors to replace it. To do so, the channel length and the channel width of each transistor in the original circuit must be resized properly and rounded off to a whole-number multiple of that of unit-transistor. In other words, the values of $l_u$ and $w_u$ are chosen carefully so that the rounding error is minimized. The steps of choosing $l_u$ and $w_u$ are summarized as follows:

  - Step 1: choose the greatest common divisor of channel length of all the transistors in the circuit as $l_u$, if, unfortunately, $l_u$ is too small, for example, even smaller than the minimum value in the design rules, we can set $l_u$ to the minimum channel length in the design rules and resize all the channel length of the original transistors with respect to $l_u$. Also we have to resize all the channels’ width to keep the channels’ $l/w$ ratios of the original transistors.

- Step 2: choose the greatest common divisor of channel width of all the transistors. However if the numbers of unit-transistors of the matched transistors are not enough to perform symmetrical/common-centroid placement, the $W$-decomposition can be doubled, i.e., $w_u$ will be set to half of its initial value.

Once $l_u$ and $w_u$ are chosen, all the transistors in the circuit can be replaced with the unit-transistors. A simple floorplanner is used to group the unit-transistors into rows, and the rows’ locations are determined as well. The floorplanner simply determines the $R/T$ ratio of each transistor subject to the total number of its unit-transistors, i.e., determines rows to be occupied and the number of unit-transistors in each row. Obviously the following equation (Eq.(4)) holds:

$$S_{UT} = R \times T_{Row}. \quad (4)$$

where $S_{UT}$ is the total number of unit-transistors of decomposed transistor, and $R$ is the total rows occupied by the transistor, and $T_{Row}$ corresponds to the number of unit-transistors assigned in each occupied row.

- **B. Determining $L/W$-Decomposition**

After the row assignment, we have to determine the connections of unit-transistors inter-row and intra-row. For example, suppose a transistor $A$, as shown in figure 14(a), is decomposed into $n$ unit-transistors by either $L$-decomposition or $W$-decomposition, and the $n$ unit-transistors can be assigned into $k$ rows if $n$ can divide exactly by $k$. $A$ will be replaced with

![GB Plots for Different L-Decomposition](image)

*Fig. 11. The Gain Bandwidth Plot of the common-source amplifier under different transistor decomposition*

![Row based unit-transistor array](image)

*Fig. 12. Row based unit-transistor array*

![A single transistor and transistor array](image)

*Fig. 13. A single transistor and transistor array*
the unit-transistor array in figure 14(b) if it’s L-decomposed, or with the array in figure 14(c).

For a transistor being both L-decomposed and W-decomposed, it can be represented by the unit-transistors in either of two ways: a horizontal-dominated way or a vertical-dominated way (see figure 15 for example), and one row is called a horizontal stage if the decomposition is in a horizontal-dominated way, or one column is called a vertical stage if the transistor is decomposed in a vertical way.

In order to simplify the connections of unit-transistors, during the floorplanning, the number of unit-transistors assigned in each row is forced either to be multiple of the unit-transistors in one stage, i.e., multiple stages in one row, or to be divided by the number of unit-transistors in one stage, i.e., one stage in multiple rows.

Please note that the horizontal-dominated decomposition is preferred since L-decomposition will increase the number of source/drain regions, thereby increasing the parasitic resistance and capacitance.

Since the ways in which the transistors are decomposed have been determined, we can use these information to generate the layout for the unit-transistors and the inner-connections of each original transistor. With such a row-based structure, it is possible to employ the placement algorithms proposed in [13] to generate a symmetric/common-centroid placement row by row. It is also quite easy to use the channel routing algorithm [11] of digital IC design to connect the unit-transistors in each row, and use the channel assignment algorithm of digital IC design to connect the transistor arrays in different rows.

D. A Simple Framework of Analog Design with Transistor Array

Given the row capacity, i.e., the maximum number of the unit-transistors that a row can hold, the framework to generate the structured analog layout with transistor array is simply summarized as follows.

- Choose \( l_u \) and \( w_u \) subject to the design rules and meanwhile minimize the routing off error.
- Assign transistors into rows (floorplanning) aiming at minimum of the total vertical wirelength (Please note that the reason we use the total vertical wirelength instead of total wirelength is that the location of the unit-transistors in each row is unknown yet).
- Determine the \( L/W \) decomposition.
- Use a constraint-driven 1-D placement algorithm to determine the sites of the transistors in each row.
- Perform channel routing/assignment for each row or the adjacent two rows using the horizontal channels.
- Perform the channel routing/assignment for inter-row connections using the vertical channels.

V. LAYOUT COMPARISON

Using the layout generation method presented in the previous section, we generate 12 layouts for a typical CMOS OPAMP circuit (figure 16), with transistor array, called TA OPAMPs. The results are compared with 6 manual design (called custom OPAMPs) in layout size, as shown in table I. It should be noted that the resistors and capacitors in both automatic design and manual design are laid out by hand, and have same layouts in all 18 OPAMPs. All the transistors of the OPAMPs are implemented in the styles of figure 13. The gray rectangles in figure 13 are dummy fingers. The unit-transistor array in the TA OPAMPs are implemented in two styles: one is with source/drain sharing, as shown in figure 13(b), the other is without source/drain sharing, as show in figure 13(c).

We choose three different channel length for the unit-transistors, i.e., \( l_u = 0.34\mu m, 0.18\mu m \) and \( 0.1\mu m \). The reason we choose these irregular values is because the effective channel lengths in the chip are slightly different from the layout. According to the process information, the effective channels are \( l_u = 0.32\mu m, 0.16\mu m \) and \( 0.08\mu m \), which exactly correspond to the channel length of non-L-decomposition, 2X-L-decomposition, and 4X-L-decomposition respectively.

Since the test chip with the eighteen OPAMPs are still under fabrication, currently, we are not able to measure the performance difference. So in this paper we only compared the layout size and design time of custom OPAMPs and TA OPAMPs. Table I shows the comparison results.
According to table I, we can see that the layout areas of TA OPAMPs with S/D sharing are about 10% to 25% (15% on average) larger than that of custom OPAMPs. But for the TA OPAMPs without S/D sharing, the layout areas are about 20% to 55% (35% on average) larger than that of custom OPAMPs. Despite the unpromising layout areas of TA OPAMPs without S/D sharing, however, given the circumstance that every two adjacent unit-transistors should meet the spacing rule, the resultant areas are reasonable and acceptable. Plus, the TA based automatic design, which includes the floorplanning, only takes about 4 seconds to finish a design. It is much faster than the manually layout synthesis. Figure 17 shows a layout example of custom OPAMP and an layout example of TA OPAMP.

VI. CONCLUSIONS AND FUTURE WORKS

This paper addresses the problem of the transistor decomposition in both channel width direction and channel length direction. The transistor decomposition and structured analog circuit design can be used in high accuracy applications. Because of the lack of the theoretical support from the well-known transistor model, we made a test chip to verify the feasibility of the transistor decomposition. The AC/DC measurement results from the chip suggests that the decomposition, as well as structured analog design based on the transistor array are applicable.

We also propose a simple structured analog layout generation framework based on the transistor array. Using this framework, we generate several layouts for a typical CMOS OPAMP circuit with the transistor array. We compared the automatically generated layouts with the manual layouts. Although the layout sizes of the transistor array based OPAMPs are larger than that of the manual designs, the automatic layout generation is much faster than manually synthesizing the layout.

Since currently the SPICE-like simulation tools are using Eq.(1) to model the transistor, we are not able to use these tools to simulate the design with L-decomposed transistors. Therefore modeling the L-decomposed transistors will be one of our future works.

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